PONTIFICIA UNIVERSIDAD CATOLICA DE CHILE
SCHOOL OF ENGINEERING

# CMOS TECHNIQUES IN INTEGRATED CIRCUITS FOR PARTICLE PHYSICS EXPERIMENTS

**ENRIQUE ALVAREZ FONTECILLA**

Thesis submitted to the Office of Research and Graduate Studies
in partial fulfillment of the requirements for the degree of
Master of Science in Engineering

Advisor:
ANGEL ABUSLEME HOFFMAN

Santiago de Chile, July 2013

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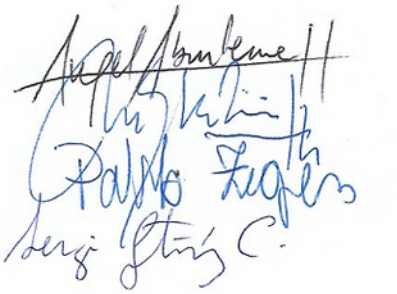

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# ABSTRACT

Particle Physics is the branch of physics that studies the fundamental subatomic particles and their properties. The main tools used by particle physicists are particle accelerators, which have multichannel detector systems around the collision point. The International Linear Collider (ILC), a next generation, 31-kilometer long particle accelerator, will smash electron and positron bunches at up to 500 GeV. Located at the ILC detector forward region, is the BeamCal, a highly segmented calorimeter. The BeamCal specifications for radiation tolerance, noise, signal charge, pulse rate and occupancy pose unique challenges for the instrumentation system.

Framed in the design, integration and testing of a 5-channel integrated circuit (IC) to address the BeamCal instrumentation needs, this thesis presents: the development of a design-oriented noise analysis technique for charge amplifiers; the design and implementation of a 10-bit fully-differential successive approximation register (SAR) analog-to-digital converter (ADC) to be included in the BeamCal instrumentation IC, along with the implementation of customized metal-oxide-metal (MOM) capacitors; and the design and implementation of a new SAR ADC architecture, which aims to minimize the energy consumed per conversion by using a passive reference-sharing algorithm.

**Keywords:** Analog-to-Digital Converter (ADC), Copper Dishing, Electronic Noise, Integral Non-Linearity (INL), Low-Noise Amplifiers, Metal-Oxide-Metal (MOM) Capacitors, Nuclear Physics Instrumentation, Passive Charge-Sharing (PCS), Passive Reference-Sharing (PRS), Successive Approximation Register (SAR).

# RESUMEN

La Física de Partículas es la rama de la física que estudia las partículas fundamentales subatómicas y sus propiedades. Las principales herramientas utilizadas por los físicos de partículas son los aceleradores de partículas, los cuales cuentan con sistemas de detectores de múltiples canales alrededor del punto donde ocurre la colisión. El Colisionador Lineal Internacional (ILC) es un colisionador de la próxima generación de 31 kilómetros de largo que colisionará grupos de electrones y positrones a 500 GeV. Ubicado en la región delantera del ILC se encuentra el BeamCal, un calorímetro altamente segmentado. Las especificaciones del BeamCal para tolerancia a la radiación, ruido, señal de carga, tasa de pulsos y ocupación plantean desafíos únicos para el sistema de instrumentación.

Enmarcado en el diseño, integración y prueba de un circuito integrado (IC) de cinco canales para satisfacer las necesidades de instrumentación del BeamCal, esta tesis presenta: el desarrollo de una técnica de análisis de ruido orientada al diseño para amplificadores de carga; el diseño e implementación de un conversor de datos análogo-digital (ADC) de aproximaciones sucesivas (SAR) completamente diferencial que será incluido en el IC de instrumentación del Beamcal, junto con la implementación de capacitores de metal-óxido-metal (MOM); y el diseño e implementación de una nueva arquitectura de SAR ADC, la cual apunta a minimizar la energía consumida por conversión utilizando un algoritmo de compartición de referencia pasivo.

**Palabras Claves:** Amplificador de Bajo Ruido, Capacitores de Metal-Óxido-Metal, Compartición de Carga Pasiva (PCS), Compartición de Referencia Pasiva (PRS), Conversor de Datos Análogo-Digital (ADC), Instrumentación para Física Nuclear, No-Linealidad Integral (INL), Planarización de Cobre, Registro de Aproximaciones Sucesivas (SAR), Ruido Electrónico.

# 1. INTRODUCTION

Particle Physics, also called High Energy Physics, is the branch of physics that studies the fundamental subatomic particles and their properties. Starting with the famous experiments by Rutherford on metal foil ion bombardment in 1909, particle physics is requiring ever-increasing energies to explore deeper into matter, as well as improved detection technology to find elusive particles and reconstruct their trajectories precisely for a better identification and understanding. In order to achieve the required energies, particles are nowadays accelerated in kilometer-scale accelerators, which are among the most ambitious engineering projects ever undertaken. Examples of these enormous instruments are the Large Hadron Collider (LHC) at Organisation Européenne pour la Recherche Nucléaire (CERN), the Tevatron at Fermilab, and the PEP-II Accelerator at SLAC National Accelerator Laboratory.

A typical modern detector system for collider (particle-particle) experiments is cylindrical shaped and includes several layers. Each layer can have thousands of pixels or channels, providing better spacial resolution and noise performance. The entire detector system is subject to a strong magnetic field provided by an enclosing magnet, which curves the path of charged particles and makes it possible to infer their momentum and charge from the radius of curvature. Only a small percentage of all particle collisions will produce the most elusive particles. To improve the odds, particle physics experiments are conducted at very high collision rates (MHz) and during very long periods (months). The beam consists of bunches of particles arranged in pulse trains, with a high pulse rate during the short, active part of the cycle, followed by a longer, silent period. Data captured from collision outcome is continuously generated by the detectors and analyzed statistically in a computer network. The study of the resulting decay products that scatter from the collision point provides information on the nature of elementary particles.

The International Linear Collider (ILC), a next generation, 31-kilometer long particle accelerator, will smash electron and positron bunches at up to $500$ GeV ($1000$ GeV after

a planned upgrade). Located at the ILC detector forward region, the BeamCal is a highly segmented ($> 90000$ channels) calorimeter that will serve three main purposes: ensure hermeticity of the detector for low polar angles, reduce the backscattering from pairs into the inner ILC detector part and protect the final magnet of the beam delivery system, and provide a low latency signal for beam diagnostics. The BeamCal specifications for radiation tolerance, noise, signal charge, pulse rate and occupancy pose unique challenges for the instrumentation system.

This thesis is part of the project FONDECYT 11110165: Application of Advanced CMOS Techniques in Pulse Processors for Particle Physics Experiments, which deals with the design and implementation of a mixed-signal integrated circuit (IC) to address the BeamCal instrumentation needs. Following, a brief description of this project is given, and the topics addressed by this thesis are specified. Then, basic notions about the subjects treated in this work are explained, and finally the thesis structure is detailed.

### 1.1. Thesis Context

Advances in electronics in the last 40 years, powered by the IC and evidenced by Moore's law, have provided a flexible tool for signal processing. The microelectronics industry has revolutionized computer engineering, telecommunications, embedded systems, control systems and bioengineering, and particle physicists have also taken advantage of these advances, with faster, more sensitive and larger instrumentation systems. The main topic of this project, and an important component of all contemporary detector systems for particle accelerators, is the front-end electronics integrated circuit, needed to acquire, filter and deliver the information of collisions captured by the detector array.

As mentioned earlier, a typical particle physics experiment detector system contains different layers of detectors, each of which is usually highly segmented into a multichannel array. A single channel of a certain layer includes a detector, an amplifier, a filter, buffers, an analog-to-digital converter (ADC), and a readout circuit (Spieler, 2005). Fig. 1.1 shows a highly simplified block diagram for a generic detector channel.

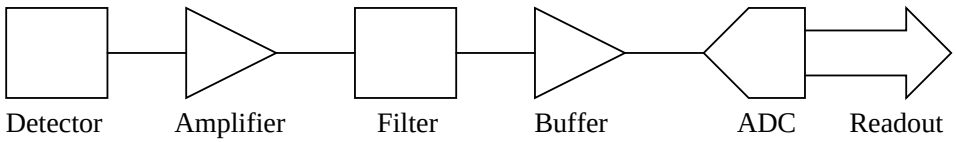



FIGURE 1.1. Block diagram for a single channel, generic instrumentation circuit for particle physics experiments.

The initial amplifier in a front-end IC for particle physics experiments translates the detector charge signal into an output voltage. Charge-to-voltage translation is done by transfering the charge $Q_{in}$ from the nonlinear capacitance of the detector to a linear, known capacitor $C$. The measured voltage $V_{out}$ is simply given by $V_{out} = Q_{in}/C$, with $C$ easily and precisely tailorable. The most common preamplifier implementation consists of a voltage amplifier with a capacitor in negative feedback configuration. The resulting feedback circuit is a CSA, extensively studied in the literature (Snoeys et al., 2000; Aspell et al., 2001; De Geronimo & O'Connor, 2005; O'Connor & De Geronimo, 1999; Alvarez et al., 2012). The amplified detector signal includes noise from the detector and the amplifier. Although the noise is a random signal in the time domain, its frequency behavior is well modeled and may be used to design a filter, also named pulse shaper, that maximizes the signal-to-noise ratio (SNR). Usually the filter is an analog block, either time-invariant (TI) or time-varying (TV), that shapes the amplified charge into a voltage pulse. The pulse shape defines the weights of white series, white parallel and flicker series noise sources on the front-end output noise. Depending on the nature of the experiment and the energies involved, only a fraction of the channels will be subject to the effect of scattered particles or photons for each collision or event. The non-excited pixels will detect and amplify noise, which is not useful for post-processing and should not be read out. In order to consider only relevant signals, threshold-based discriminators are typically used. A memory acts as a buffer necessary to store data for a number of events before readout. For high-frequency pulse trains, analog memory is particularly well suited (Kleinfelder et al., 2004; Haller & Wooley, 1994). Filtered signals can be quickly stored as charge in integrated metal-insulator-metal (MIM) or metal-oxide-semiconductor (MOS) capacitors, to be converted

into digital signals by dedicated analog-to-digital converters during the readout phase. Integration and feature size reduction has allowed the design of highly dense digital memory arrays. If a digital memory is used instead, ADCs are used to digitize the signal prior to storage, and conversion throughput per IC must be as high as the collision rate times the number of channels. This can be done using a single, fast ADC shared among a number of channels, or several slower ADCs.

### 1.1.1. Project Brief

Specifically, the work proposed on this project is the design, integration and testing of a mixed-signal IC to address the BeamCal instrumentation needs. A 5-channel IC, based on the 3-channel prototype developed in a previous work (Abusleme, 2011), will be designed for a $0.18$-$\mu$m CMOS process. Each independent channel will include: a charge-sensing amplifier (CSA) with a precharging pulser; a fully differential switched-capacitor (SC) filter with a low-frequency noise suppression feature; a buffer; a 10-bit, fully-differential, successive approximation register (SAR) analog-to-digital converter (ADC); and a digital storage array. Additionally, the IC will feature a fast feedback adder for beam diagnostics purposes. The IC will be capable of processing the BeamCal detector output at the ILC nominal frequency of $3.2468$ MHz, with $100\%$ occupancy. A power-cycling feature will ensure a low power consumption. The IC to be developed will represent an improvement over the previous version. In the new prototype, improvements include additional channels, a digital memory array, a more effective low-frequency noise suppression mechanism, and a power-cycling feature. In order to reduce the ADC power consumption and input capacitance, the SAR ADC will employ a capacitor array made of small metal-oxide-metal (MOM) capacitors. The IC testing and characterization will be done in two stages. During the first stage, the IC will be tested for a simulated detector, using an idealized pulser capable of injecting a controllable, known charge. In a second stage, the IC will be placed in an actual beamline at the Deutsche Elektronen-Synchrotron (DESY), Zeuthen, for a more realistic operating condition.

The main goal of this project is to prove that advanced CMOS circuit design techniques, such as SC circuits and ADCs based on MOM capacitors, can be used effectively to address the instrumentation requirements in particle physics experiments. During the development of this project, the classic noise minimization techniques (minimum transistor size, maximum power available, and independence of filter time constant on flicker noise contribution) will be questioned, particularly in the context of modern CMOS devices. Also, this work attempts to explore further into the practical limits of MOM capacitors matching. The outcome of this research may lead to power-efficient ADC converters with an extremely low input capacitance, which can be also scaled down on newer technologies.

### 1.1.2. Topics Covered by the Thesis

As mentioned earlier, besides the design, implementation and testing of the BeamCal instrumentation IC, one of the aims of this project is to question the classical noise minimization techniques, which can be done by developing design-oriented analysis techniques capable of providing the information necessary to corroborate the classical approach validity. Particularly, in this thesis a new approach on noise analysis for charge amplifiers based on an extension of the $g_m/I_D$ technique is presented. The method, which allows to find the optimal operation point of the charge amplifier input device for maximum resolution, states new design considerations for noise minimization, and also provides a deeper insight on the noise limits mechanism from an alternative and more design-oriented point of view[1].

The design and implementation of the 10-bit fully-differential SAR ADC to be included in the BeamCal instrumentation IC are also covered by this work, along with the implementation of custom MOM capacitors. The implemented ADC features a power-saving state and non-linearitiy correction, which aims to cancel out the charge amplifier non-linearity. Moreover, this thesis presents a new SAR ADC architecture, which aims

[1] See the related publications (Alvarez & Abusleme, 2012; Alvarez et al., 2012).

to minimize the energy consumed per conversion by using a passive reference-sharing algorithm. This novel architecture allows for a capacitance spread of one, a small area, a low-power consumption and a reconfigurable resolution.

## 1.2. Basic Notions

In this section, a brief review on some of the topics treated throughout this work is presented. The topics covered are noise in electronics circuis, differential and integral nonlinearity of ADCs, and the successive approximation algorithm. The scope of this section is merely introductory, intended for readers with no background in the topics treated in this thesis.

### 1.2.1. Noise in Electronics

In electronics, noise is a random fluctuation in an electrical signal, and is present in all electronic circuits. It constitutes an important issue in the design of integrated circuits, since it affects the accuracy of the signals processed. Noise generated by electronic devices, such as bipolar transistors and MOSFETs, varies greatly, as it can be produced by several different physical processes. There are three sources of fundamental noise in MOSFETs (Gray et al., 2001): shot noise due to gate leakage current, thermal (for strong inversion operation) or shot (for weak inversion operation) noise in the channel, which is always white, and flicker or $1/f$ noise, also called low-frequency noise. These noise sources have been widely studied throughout the years, and several works about them can be found in the literature. References (Gray et al., 2001; Jindal, 2006) are good start points for introducing the reader into this subject.

Noise is naturally expressed as a frequency-dependent power spectral density, in either $V^2/Hz$ or $A^2/Hz$. The integral of the noise power spectrum over the circuit bandwidth yields the total circuit noise power, and its square root is the standard deviation of either the noise voltage or noise current.

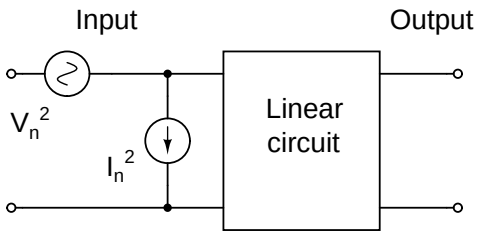



FIGURE 1.2. Equivalent representation of a linear circuit internal noise sources, referred to the input port.

In an electronic circuit, composed by a number of electronic devices, there are several noise sources. To quantify the effect of these different noise sources, each one of them can be referred to a common node of the circuit, typically the input node. Noise sources referred to the same node are added as power as follows

$$\sigma^2_{Total} = \sigma^2_1 + \sigma^2_2 + 2 \cdot c \cdot \sigma_1 \cdot \sigma_2 \tag{1.1}$$

where $\sigma^2_i$ represents the noise power of source $i$, and $c$ is the correlation coefficient between the two noise sources. If both noises come from the same physical process (i.e., they are fully correlated), $c = 1$ and $\sigma_{Total} = \sigma_1 + \sigma_2$ is given by the sum of the noise signals; if the noises come from different noise sources, they are usually not correlated ($c = 0$) and $\sigma^2_{Total} = \sigma^2_1 + \sigma^2_2$ is the given by the sum of individual powers.

By referring the noise sources to the input of the system, it is possible to make a fair comparison of noise performance among different systems with different gains, and set the total input-referred noise as a figure of merit. In a linear circuit, the total input-referred noise can be represented by a combination of a series voltage noise source ($V^2_n$) and a parallel current noise source ($I^2_n$), as shown in Fig. 1.2. If the driving signal is a low-impedance voltage source, only the voltage noise is important, whereas if the signal source is a high-impedance current source, the voltage noise can be neglected, as current noise accounts for all the system noise. In system with a non-ideal load line, both noise sources must be considered.

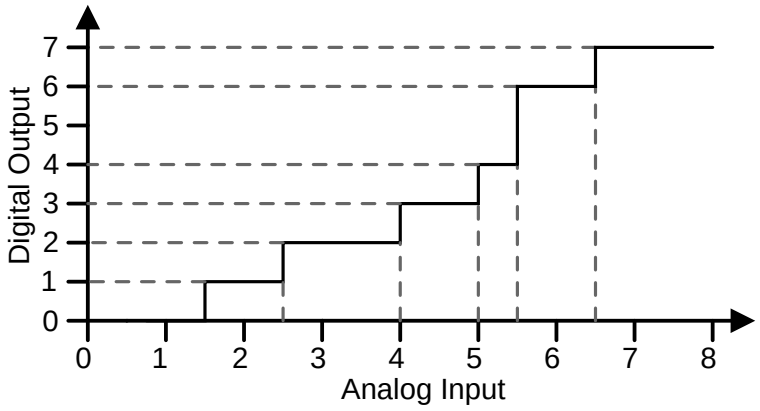



FIGURE 1.3. 3-bit ADC transfer function.

### 1.2.2. DNL and INL

Analog-to-digital converters convert continuous analog signals into a discrete digital representation. There are many different specifications used to characterize the performance of an ADC. Particularly, there are two specifications that will be treated extensively in this document, the differential non-linearity (DNL) and the integral non-linearity (INL) (Maloberti, 2007). Both are static performance metrics, this is, they are valid for DC input signals.

#### Differential Non-Linearity

Ideally, every code of an ADC should have the same width[2], and any two adjacent digital codes should correspond to two analog voltages that are exactly one LSB (Least Significant Bit) apart. In practice this does not necessarily hold, and there are wider codes and narrower codes. The $DNL(k)$ is a vector that represents, for each code $k$, its deviation from its ideal width, and is measured in LSBs. The $DNL$ of the $k$-th code is defined as

$$DNL(k) = \frac{W_k - W_{ideal}}{W_{ideal}} \tag{1.2}$$

where $W_k$ is the $k$-th code width and $W_{ideal}$ is the codes ideal width.

[2]The width of a code is defined as the input signal range that corresponds to that code in the converter static transfer characteristic.

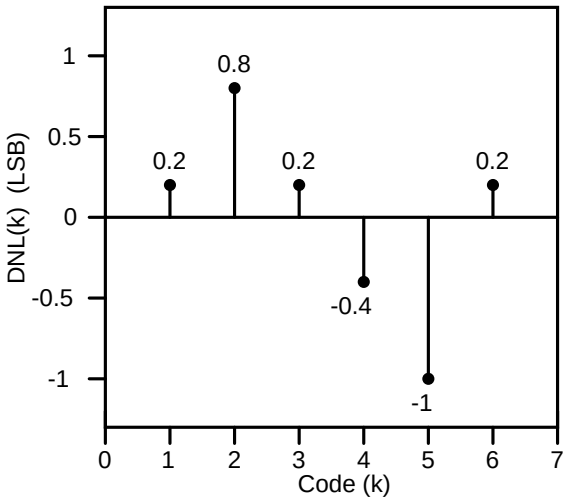



FIGURE 1.4. 3-bit ADC DNL.

As an example, let us consider a 3-bit ADC with the transfer function depicted in Fig. 1.3. The codes of the edges (codes 0 and 7) have an undefined width, so $DNL(0)$ and $DNL(7)$ are also undefined. To compute $W_{ideal}$, the range between the first and the last transition must be divided into $2^B - 2$ equal parts, where $B$ is the number of bits, then

$$W_{ideal} = \frac{6.5 - 1.5}{2^3 - 2} = \frac{5}{6}. \tag{1.3}$$

According to Fig. 1.3, the codes widths are given by $W_1 = 1$, $W_2 = 1.5$, $W_3 = 1$, $W_4 = 0.5$, $W_5 = 0$ and $W_6 = 1$. Fig. 1.4 shows the DNL of the 3-bit ADC. It can be observed that $DNL = -1$ implies that the code is missing, and that $\sum_{k=1}^{6} DNL(k) = 0$. Usually, the maximum and minimum values of $DNL(k)$ for an ADC are reported. For instance, $DNL = +0.8/-1$.

**Integral Non-Linearity**

The integral non-linearity (INL) is a measure of how closely the ADC output matches its ideal response, and is usually defined as the deviation in LSBs of the actual transfer function of the ADC from a straight line passing through the end-points (first code and last code), which corresponds to the ideal transfer curve (see Fig. 1.5).

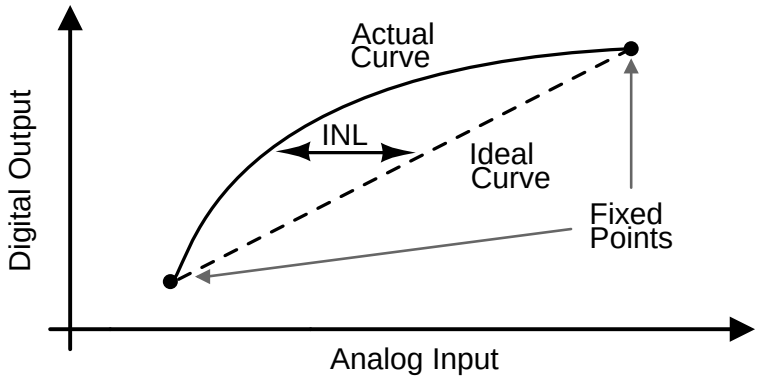



FIGURE 1.5. Illustration of the integral non-linearity of an ADC.

The $INL$ of the $k$-th code is defined as follows

$$INL(k) = \frac{T_k - T_{k,ideal}}{W_{ideal}} \tag{1.4}$$

where $T_k$ is the $k$-th code actual transition and $T_{k,ideal}$ is the $k$-th code ideal transition. The ideal transitions must be computed by dividing the range between the first and the last transition into $2^B - 2$ equal parts. In the example of Fig. 1.3, the ideal transitions are given by $T_{k,ideal} = 1.5 + k \cdot 5/6$.

Fig. 1.6 shows the INL of the 3-bit ADC of the previous example. Since the end-points are fixed, $INL(1) = 0$ and $INL(7) = 0$. Also, $INL(0)$ is not defined. It can be shown that $INL(k)$ can be defined as the cumulative sum of $DNL(k)$, i.e., $INL(k) = \sum_{i=1}^{k-1} DNL(i)$. Usually, the maximum and minimum values of $INL(k)$ for an ADC are reported. For instance, $INL = +1.2/-0.2$.

### 1.2.3. Successive Approximation Algorithm

Since both ADCs covered by this thesis are successive approximation register (SAR) charge-redistribution ADCs, the basic principle of operation of this type of converter architecture should be first reviewed. This section aims to clarify the mathematical algorithm behind a SAR ADC operation.

A successive approximation ADC is a type of analog-to-digital converter that converts a continuous analog signal into a discrete digital representation via a binary search. The

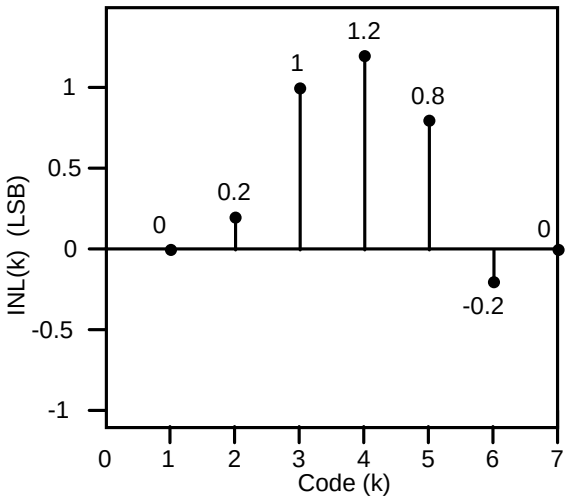



FIGURE 1.6. 3-bit ADC INL.

algorithm used by this type of converter works as follows: given an analog input signal $v_{in}$ bounded to $\pm V_r$, the $B$-bit digital representation is obtained by adding or subtracting, step by step, binary scaled fractions of $V_r$ (i.e., $V_r/2$, $V_r/4$, $V_r/8$, ... $V_r/2^{B-1}$) to the input signal. Depending on the sign of the result obtained at each step, each bit of the $B$-bit digital output is determined. More specifically, if $v_{in} > 0$, the most significant bit (MSB) $B_1$ is set to 1 and the signal to be evaluated at the next step is determined as $v_2 = v_{in} - V_r/2$, whereas if $v_{in} < 0$, $B_1 = 0$ and $v_2 = v_{in} + V_r/2$. Then, at the second step, the sign of $v_2$ is evaluated, the second MSB $B_2$ is determined and $v_3 = v_2 \pm V_r/4$. At the $i$-th step, the sign of $v_i$ is evaluated, $B_i$ is determined and $v_{i+1} = v_i \pm V_r/2^{i-1}$. This process continues until the least significant bit (LSB) is determined.

Fig. 1.7 shows four examples of binary search for a signal $v_{in}$ bounded to $\pm 8$ and a 4-bit digital output. For example, for $v_{in} = -1.5$ (see top right corner of Fig. 1.7), at the first step, the MSB $B_1$ is set to 0, and the signal to be evaluated at the next step is determined as $v_2 = -1.5 + 8/2 = 2.5$. At the second step, $B_2$ is set to 1 (since $v_2 > 0$) and $v_3$ is determined as $v_2 = 2.5 - 8/4 = 0.5$. At the third step, $B_3$ is set to 1 ($v_3 > 0$) and $v_4$ is determined as $v_4 = 0.5 - 8/8 = -0.5$. Finally, at the fourth step, the LSB $B_4$ is set to 0 ($v_4 < 0$) and the conversion finishes.

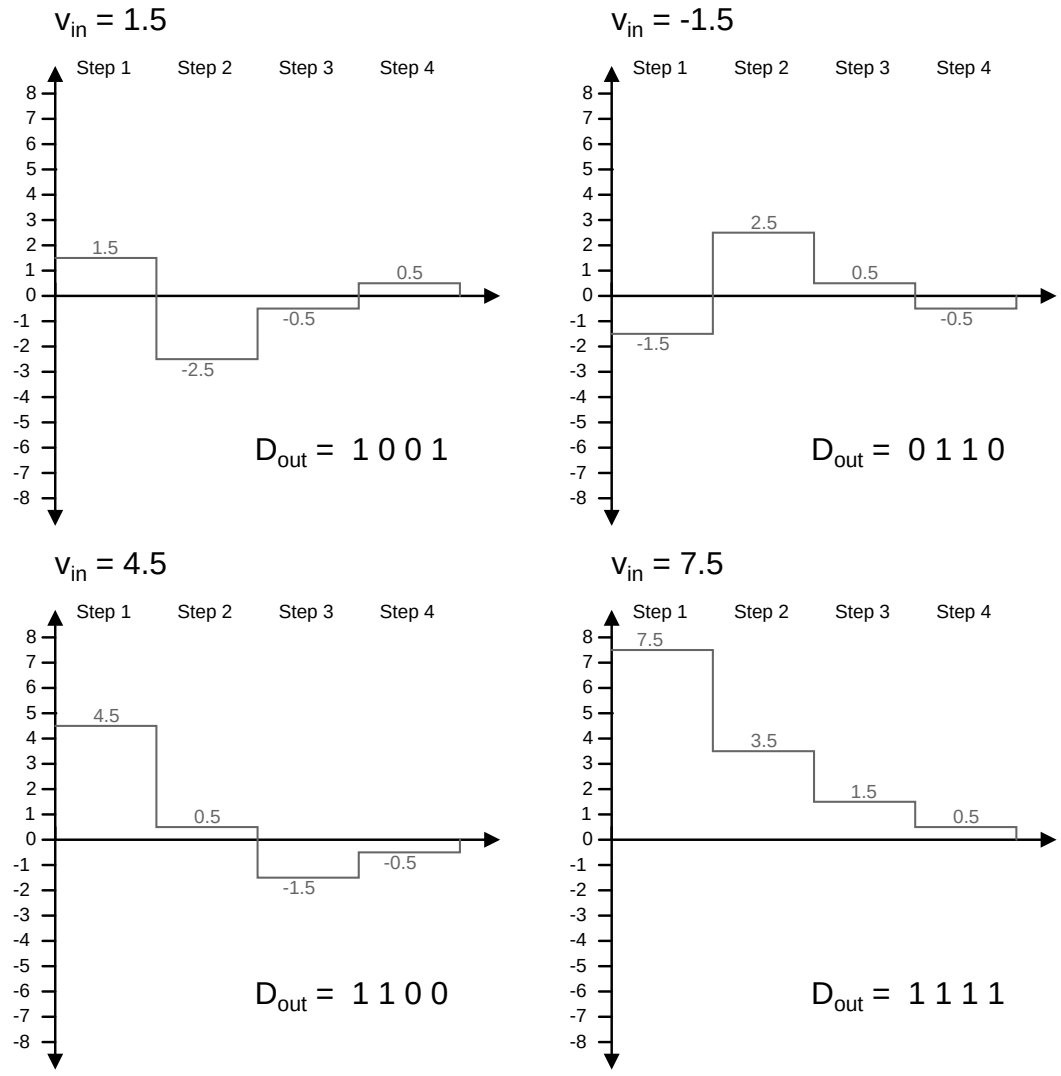



FIGURE 1.7. Successive approximation algorithm illustrated step by step for four different input values. The input signal $v_{in}$ is bounded to $\pm 8$, and the digital output has four bits.

Now that the basic notions required to introduce the reader to the topics treated throughout this thesis have been covered, in the next section, the thesis contents are briefly revised.

## 1.3. Thesis Structure

Chapter 2 presents an approach on noise analysis for charge amplifiers based on an extension of the $g_m/I_D$ technique, Chapter 3 details the design of the SAR ADC to be

included in the BeamCal instrumentation IC, and Chapter 4 presents a reconfigurable, fully-differential, low-power, passive reference voltage sharing SAR ADC architecture. In Chapter 5 the results obtained from experimental testing are presented, and finally, in Chapter 6, the conclusions are drawn.

# 2. NOISE IN CHARGE AMPLIFIERS – A $G_M/I_D$ APPROACH

Charge amplifiers represent the standard solution to amplify signals from capacitive detectors in high energy physics experiments. In a typical front-end, the noise due to the charge amplifier, and particularly from its input transistor, limits the achievable resolution. The classic approach to attenuate noise effects in MOSFET charge amplifiers is to use the maximum power available, to use a minimum-length input device, and to establish the input transistor width in order to achieve the optimal capacitive matching at the input node. These conclusions, reached by analysis based on simple noise models, lead to sub-optimal results. In this chapter, a new approach on noise analysis for charge amplifiers based on an extension of the $g_m/I_D$ methodology is presented. This method combines circuit equations and results from SPICE simulations, both valid for all operation regions and including all noise sources. The method, which allows to find the optimal operation point of the charge amplifier input device for maximum resolution, shows that the minimum device length is not necessarily the optimal, that flicker noise is responsible for the non-monotonic noise versus current function, and provides a deeper insight on the noise limits mechanism from an alternative and more design-oriented point of view.

## 2.1. Introduction

Noise sets a fundamental limit on the resolution in measurements for particle physics experiments and radiation detectors. In a typical front-end circuit, consisting of a charge amplifier and a filter, the former is responsible for most of the noise present in the readout circuit signal path (De Geronimo et al., 2001; De Geronimo & O'Connor, 2005). Thus, a proper, integral design of the front-end for a particular detector ensures an adequate noise behavior (Sansen & Chang, 1990).

Noise analysis for particle physics circuits is usually carried out by combining simple device noise models (Gray et al., 2001; Razavi, 2002) and the frequency response of the

amplifier and the filter network (Spieler, 2005). The noise analysis outcome is the equivalent noise charge (*ENC*), measured in electrons, which represents the charge required at the detector to produce an output SNR of 1. Typically the input signal is a step of charge, or equivalently, a delta pulse of current with an area equal to the charge, and consequently the charge amplifier output voltage is also a step. The filter, commonly referred to as pulse shaper, attenuates low and high frequencies, producing a time domain pulse. The signal is measured at the pulse peak, and noise is integrated over all frequencies to compute the *ENC*.

An interesting analysis methodology, presented in (Goulding, 1972; Radeka, 1988), is commonly used to simplify noise computation. The idea is to use the noise power spectral densities of the input device and detector (easy to compute due to the simplicity of noise equations) and tabulated results for the filter frequency behavior, conveniently pre-integrated and expressed as dimensionless numbers. This widely exploited technique allows a simple, insightful noise analysis, appropriate for design.

Typically, the low noise front-end design is achieved by following a simple recipe for the input transistor of the charge amplifier: maximum available current, optimal capacitance matching at the input node (which depends on the operation region) (O'Connor & De Geronimo, 1999), and minimum-length input device (Sansen & Chang, 1990; Radeka, 1984). These guidelines, obtained from analysis on simple transistor noise models and neglecting flicker noise, produce acceptable but sub-optimal results, and fail to explain why minimum noise is not a monotonically decreasing function of the input transistor current.

Using more adequate models for current technologies and wider inversion coefficient range, in (De Geronimo & O'Connor, 2005) the authors show that the guidelines previously stated do not necessarily produce optimal results, and conclude that flicker noise is responsible for the noise lowest limit. In (Gryboś et al., 2006), simplified EKV models were used to find several novel aspects of noise optimization for charge amplifiers. Both innovative ideas base their analysis on more realistic – and more complex – equations for the input transistor noise.

A new noise analysis technique, presented in this chapter, is as follows: noise power spectral densities for a set of transistors are pre-computed by means of SPICE simulations, using the most comprehensive noise models available. The resulting curves are then properly scaled for the appropriate device parameters using the $g_m/I_D$ technique (Silveira et al., 1996; Flandre et al., 1997), conveniently modified to include noise. Finally, noise power spectral density can be obtained by using simple interpolations within the curves and the *ENC* can be integrated numerically. The main advantage of this approach is that it allows to work with simple and insightful analytical expressions, appropriate for design-oriented analysis.

This precise noise analysis technique can be used for the input-referred amplifier noise, either considering only the input device – in any operation region – or the noise contributions of more devices in the amplifier. Compared to previous methods, this one provides a better insight on the noise contributions by means of noise charts, adequate for a design process. The methodology was used to explore the design space of a charge amplifier for particle physics experiments, allowing to reach and complement the conclusions from (De Geronimo & O'Connor, 2005) regarding flicker noise contribution.

Without compromising the validity of the analysis only the preamplifier input device noise contribution will be considered, and generic BSIM3 noise models will be used. In real applications, secondary noise sources should be considered (Fabris & Manfredi, 2002) as well as model parameters validated by measurements.

## 2.2. The $g_m/I_D$ Methodology and Noise Analysis

The evolution of MOSFET models for deep submicron technologies has improved the accuracy of SPICE simulation results. However, the equations have become non practical for hand calculations, and the use of simple equations leads to inaccurate results. Although the $g_m/I_D$ methodology overcomes this limitation using accurate SPICE simulation results as data for hand analysis (Silveira et al., 1996; Flandre et al., 1997), this methodology does not state clearly how to deal with noise analysis. An application for

the use of the $g_m/I_D$ methodology for noise analysis was later developed (Ou, 2011), but the procedure relies on extracting two noise parameters instead of a detailed curve of noise over frequency, and does not provide an insight on the dependence of noise on the $g_m/I_D$ parameter. A new noise analysis technique, presented in this section, attempts to overcome this limitation. Noise curves for a set of transistors are pre-computed by means of SPICE simulations, using the most comprehensive noise models available. The curves are then properly scaled for the appropriate device parameters using the $g_m/I_D$ technique, conveniently modified to include noise. Finally, noise can be computed by using simple interpolations within the curves.

Consider a transistor biased at a certain operation point, with a drain current $I_D$ and an overdrive voltage $V_{OV}$. If another transistor with the same parameters and bias is connected in parallel, the compound transistor will have the following variables doubled in magnitude: drain current ($I_D$), effective width ($W$), gate-to-source capacitance ($C_{gs}$) and transconductance ($g_m$). The overdrive voltage $V_{OV}$ and the level of inversion in the channel remain unchanged. The ratio $g_m/I_D$ also remains constant, and is a measure of the operation point of the transistor. Large values of $g_m/I_D$ are related to subthreshold and weak inversion operation (low overdrive voltage), whereas small values are related to strong inversion operation (high overdrive voltage). It can be shown that the transconductance efficiency is $g_m/I_D = 2/V_{OV}$ in strong inversion, and $g_m/I_D = q/nkT$ in weak inversion, where $q$ is the electron charge, $n$ is a dimensionless parameter, $k$ is the Boltzmann constant and $T$ is the absolute temperature (Laker & Sansen, 1994). Other ratios that can be mapped to the operation point are the transistor transit frequency $f_T$, usually defined as $g_m/C_{gs}$, and the current density $I_D/W$. As an example, Fig. 2.1 shows the dependence of $I_D/W$ on $g_m/I_D$ for different transistor lengths for an NMOS device in a 0.18-$\mu m$ technology, obtained via SPICE simulations. Likewise, sets of curves such as $C_{gs}/W$, $f_T$, $V_{th}$ and $V_{OV}$ as functions of $g_m/I_D$ can be easily obtained for any technology. Unfortunately, the transistor noise does not depend directly on $g_m/I_D$, thus the corresponding curves cannot be represented in this fashion.

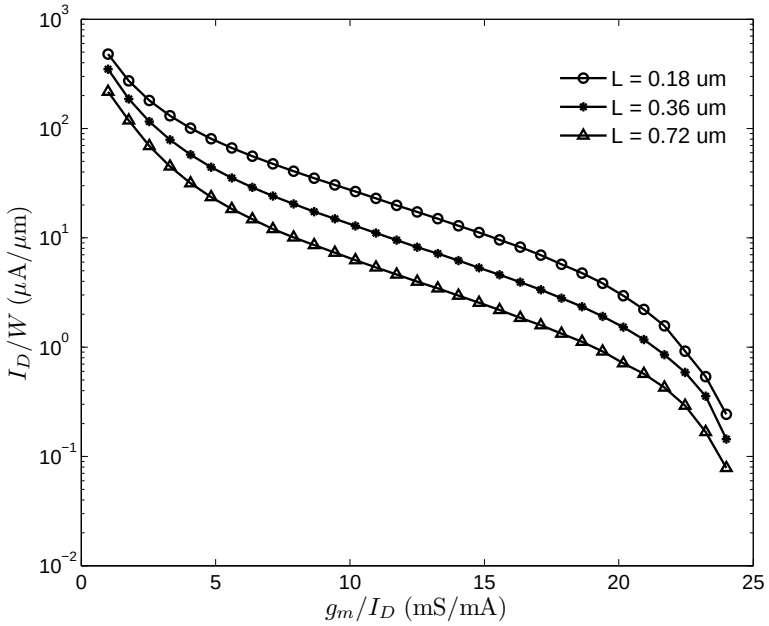



FIGURE 2.1. $I_D/W$ vs. $g_m/I_D$ for different transistor lengths. The curves were obtained using the BSIM3 MOSFET model.

As mentioned earlier, when two transistors in the same bias condition are connected in parallel, $g_m/I_D$ remains constant, but the drain current noise power ($I_n^2$) is doubled. If we want to reach a noise quantity that does not vary when $g_m/I_D$ remains constant, we need to divide the drain current noise power by any quantity that is doubled in the compound transistor, e.g. by $I_D$, $g_m$ or $W$. Thus, MOSFET noise can be expressed as a function of $g_m/I_D$ by doing a simple normalization, this is, by dividing the transistor drain current noise power spectral density by the drain current. For a certain channel length and operation point, the normalized noise power spectral density ($\hat{I}_n^2$) depends only on the technology, and can be easily obtained from SPICE simulations using models with arbitrary complexity. Later in a circuit design stage, lookup tables allow retrieving the required values for denormalization, to be used in simple hand calculations. The noise power referred to the transistor gate voltage ($V_n^2$) can also be normalized ($\hat{V}_n^2$) by multiplying it by the drain current, and can also be obtained by dividing $\hat{I}_n^2$ by $(g_m/I_D)^2$.

The dependence of the normalized noise on $g_m/I_D$ has been confirmed for different noise equations that model thermal, shot and flicker noise, including the equations used in

the BSIM3v3 models. Table 2.1 presents some examples of noise equations (Razavi, 2002; W. Liu et al., 2005; *Star-Hspice Manual*, 2001) and their normalized versions, where $W_A$ and $W_B$ are constants, and the other terms of each equation can be found in (W. Liu et al., 2005). It can be shown that the term $g_m/|Q_{inv}|$ depends on $g_m/I_D$, therefore, it is clear that all normalized noise equations depend only on $g_m/I_D$. Even though flicker noise can be further explained by several processes and modeled accordingly (Tian & El Gamal, 2001; Vandamme & Hooge, 2008), this work aims to provide a design-oriented methodology for which the specific models used are not relevant, so the circuit designer does not have to deal with the complexity of the equations.

It can be seen that the denominator of the BSIM3 equation for thermal noise has the term $g_m R_{DS}$, which is the transistor intrinsic gain, dependent on $g_m/I_D$ and $V_{DS}$. The dependence on $V_{DS}$ was added later in the BSIM model to make it more accurate, but at least as a first-order approximation the equation works for the normalization. However, if more accurate curves were necessary, several noise simulation can be done for different values of $V_{DS}$.

Fig. 2.2 shows the transistor gate voltage noise power spectral density $\hat{V}_n^2$ for different values of $g_m/I_D$ in a 0.18-$\mu m$ technology. Low values of $g_m/I_D$ imply large values of the corner frequency $\omega_c$, which corresponds to the frequency at which the white and $1/f$ components of noise are equal. This is because when $g_m/I_D$ decreases, as shown in Fig. 2.1, the $I_D/W$ ratio increases and – for constant bias current – $W$ decreases; as a consequence of a reduced gate area, flicker noise dominance extends to higher frequencies. Normalized noise provides an intuitive interpretation of noise representing it as a function of $g_m/I_D$ and the frequency, and can be easily extended to represent more complex noise models, such as those that depend on the drain-to-source voltage.

## 2.3. Noise in Pulse Processor for Particle Physics Experiments

Fig. 2.3 shows a simplified, small-signal schematic of a typical front-end circuit for particle physics experiments. The detector is presented as a capacitance $C_D$, whereas the

TABLE 2.1. Normalized noise equations.

| | $I_n^2$ | $\hat{I}_n^2$ |
|---|---|---|
| Thermal noise for strong inversion | $4k_BT\gamma g_m$ | $4k_BT\gamma\left(\frac{g_m}{I_D}\right)$ |
| Shot noise for weak inversion | $2qI_D$ | $2q$ |
| HSPICE $1/f$ noise (`NLEV=0`) | $\frac{K_F I_D^{A_F}}{C_{ox}L^2 f}$ | $\frac{K_F I_D^{A_F-1}}{C_{ox}L^2 f}$ |
| HSPICE $1/f$ noise (`NLEV=2,3`) | $\frac{K_F g_m^2}{C_{ox}WLf^{A_F}}$ | $\frac{K_F}{C_{ox}Lf^{A_F}}\left(\frac{g_m}{I_D}\right)^2\left(\frac{I_D}{W}\right)$ |
| BSIM3 thermal noise | $\frac{4k_BT}{R_{DS}+L^2/(\mu\lvert Q_{inv}\rvert)}$ | $\frac{4k_BT}{g_mR_{DS}+L^2g_m/(\mu\lvert Q_{inv}\rvert)}\left(\frac{g_m}{I_D}\right)$ |
| BSIM3 $1/f$ noise for strong inversion | $\frac{k_BT}{L^2f^{E_F}}\left(\frac{q^2\mu I_D W_A}{C_{ox}}+\frac{I_D^2\Delta L_{clm}W_B}{qW}\right)$ | $\frac{k_BT}{L^2f^{E_F}}\left(\frac{q^2\mu W_A}{C_{ox}}+\frac{\Delta L_{clm}W_B}{q}\left(\frac{I_D}{W}\right)\right)$ |

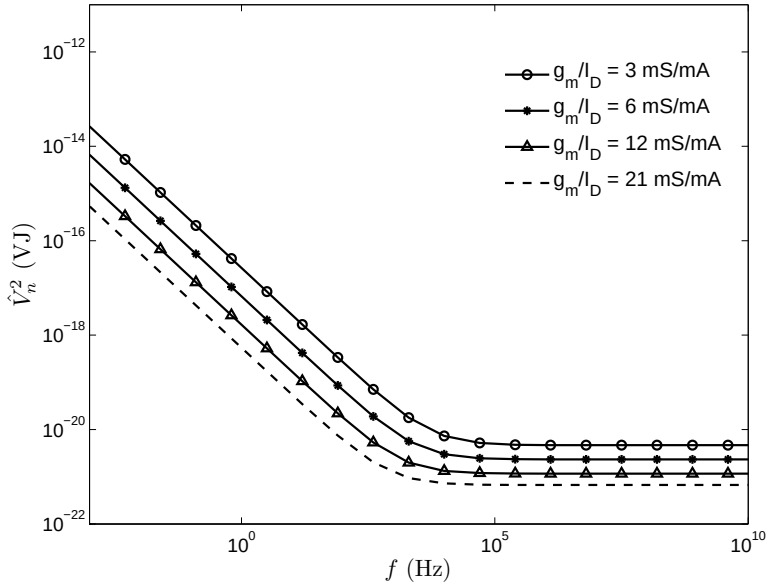



FIGURE 2.2. $\hat{V}_n^2$ vs. frequency for different values of $g_m/I_D$ and $L = 0.18\ \mu m$. The curves were obtained using the BSIM3 MOSFET model.

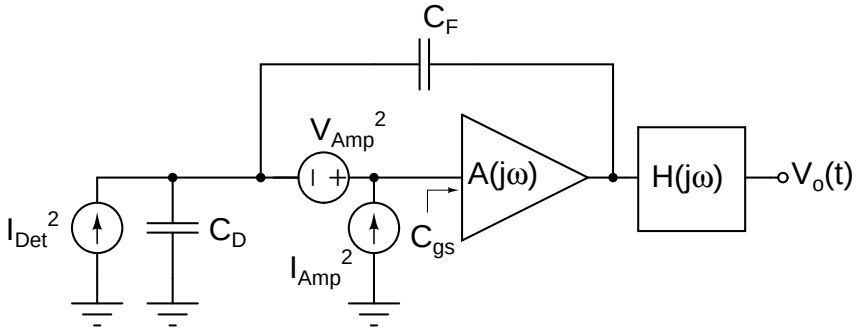



FIGURE 2.3. Schematic for noise analysis. Two noise sources are considered: detector shot noise and amplifier noise, represented as voltage and current noise; this includes both, white and flicker noise.

charge amplifier is shown as a voltage amplifier with open loop transfer function $A(j\omega)$, input capacitance $C_{gs}$ and feedback capacitor $C_F$. Detector shot noise and amplifier voltage and current noise sources are included.

The *ENC* of the circuit in Fig. 2.3 can be computed as the square root of the ratio between the total output noise power and the output power produced by the charge of a single electron in a noiseless equivalent circuit. Since the detector shot noise depends only on the pulse shaper parameters, and here it is assumed that these parameters have

been already defined through other constraints (e.g. by the maximum allowed integration time), $I_{Det}^2$ will not be considered in the *ENC*$^2$ calculation.

Defining $C_K = C_D + C_F$, and $x = g_m/I_D$, the front-end output noise $V_{o,n}^2$, considering the amplifier noise ($V_{Amp}^2$ and $I_{Amp}^2 = \omega^2 C_{gs}^2 V_{Amp}^2$), can be expressed as:

$$V_{o,n}^2 = \int_0^\infty \frac{\left(C_{gs}(x) + C_K\right)^2 \cdot |H(j\omega)|^2 \cdot V_{Amp}^2}{2\pi \cdot C_F^2} \, \mathrm{d}\omega. \tag{2.1}$$

The computed *ENC*$^2$ is shown in (2.2), where $q$ is the electron charge and $g(t)$ is the step response of $H(j\omega)$.

$$ENC^2 = \int_0^\infty \frac{\left(C_{gs}(x) + C_K\right)^2 \cdot |H(j\omega)|^2 \cdot V_{Amp}^2}{2\pi \cdot q^2 \cdot \left|\max[g(t)]\right|^2} \, \mathrm{d}\omega \tag{2.2}$$

Since the denominator of (2.2) is constant for given filter parameters, minimizing the *ENC* is equivalent to minimizing the numerator. Finally, the amplifier noise can be written as $V_{Amp}^2 = N(x,\omega)/I_D(x)$, where $N(x,\omega)$ corresponds to the total input-referred normalized noise power. Therefore, the objective function to minimize can be expressed as:

$$F_o = \frac{\left(C_{gs}(x) + C_K\right)^2}{I_D(x)} \int_0^\infty |H(j\omega)|^2 \cdot N(x,\omega) \, \mathrm{d}\omega. \tag{2.3}$$

The units of $F_o$ are irrelevant for the purposes of this work, so they will be omitted.

## 2.4. *ENC* Minimization

We will develop a brief example of *ENC* minimization for a charge amplifier design on a 0.18-$\mu m$ technology. Let us consider a CR-RC filter, with a step response given by (2.4), where $\tau_p$ is the peaking time. The equation is normalized, so that the peak amplitude of its impulse response is 1:

$$g(t) = \frac{t}{\tau_p} e^{1 - t/\tau_p}. \tag{2.4}$$

In order to compute $ENC^2$ as a function of $I_D$ for different values of $x$ and $L$, the magnitude of the filter transfer function must be computed first, and then introduced into (2.3).

Fig. 2.4 shows $F_o$ as a function of $I_D$ for $L = 0.18\ \mu m$, $K_F = 2 \cdot 10^{-29}$ and a wide range of $x$[1]. Several conclusions can be drawn from this plot. For a constant $x$, $L$ and filter parameters, the integral of (2.3) is constant, so minimizing $F_o$ is equivalent to minimizing the function

$$\begin{aligned} F_{o2} &= \frac{(C_{gs}(x) + C_K)^2}{I_D(x)} \\ &= \frac{C_{gs}}{I_D}(x) \cdot C_{gs}(x) \left(1 + \frac{C_K}{C_{gs}(x)}\right)^2 \end{aligned} \tag{2.5}$$

where $C_{gs}/I_D$ is constant for a constant $x$. Hence, there is an optimal current for which total noise due to the amplifier is minimized. The optimal current value is that for which the condition $C_{gs} = C_K$ holds. On the other hand, for a constant current, the condition of capacitance matching at the front-end amplifier does not hold anymore for the point at which the total noise is minimized. Additionally, it can be observed that the minimum noise is not a monotonically-decreasing function of $I_D$, and this can be explained as follows: as shown in Fig. 2.4, low values of $x$ produce v-shaped curves at the right of the plot, so as the current increases, each point of the minimum envelope corresponds to an operation point with a lower value of $x$ than the previous point. As explained before, low values of $x$ are related to high values of $\omega_c$, thus, flicker noise becomes dominant when increasing the current and consequently the minimum envelope is not a monotonically-decreasing function of $I_D$. This fact can also be checked by extracting normalized power noise curves without considering flicker noise (i.e., setting $K_F = 0$ in the MOSFET SPICE models) and plotting the same curves as in Fig. 2.4. The results, presented in Fig. 2.5, show that, without the presence of flicker noise, the minimum envelope is a monotonically-decreasing function of $I_D$.

Further conclusions can be drawn by analyzing the minimum noise envelope for different channel lengths, as shown in Fig. 2.6. As it can be seen, using a minimum-length

[1]Generic 0.18-$\mu m$ transistor models available at MOSIS website (*MOSIS*, 2013) were used for this work. The value of $K_F$ was selected so that the corner frequency is about 5 $MHz$.

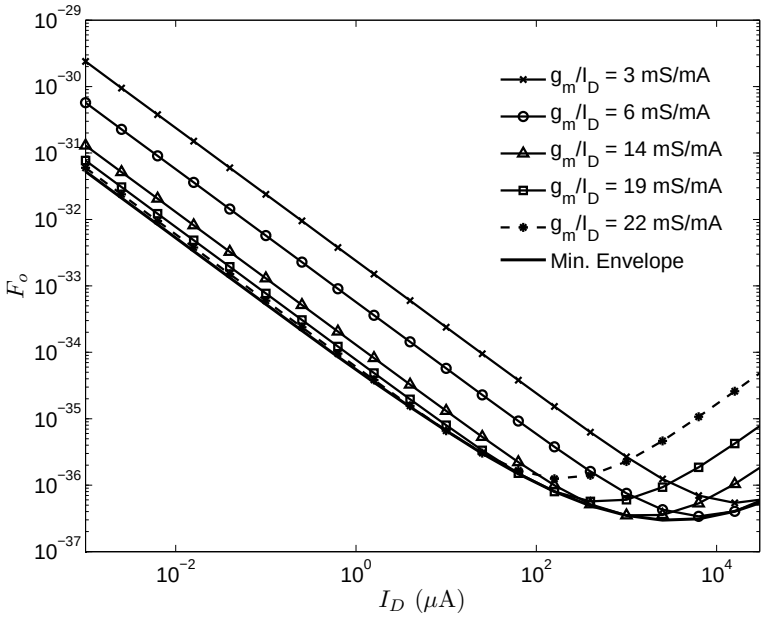



FIGURE 2.4. $F_o$ as a function of $I_D$ for different operation points. The input device optimal operation point is at $x^* = 10.2$ mS/mA.

input device does not necessarily represent the optimal solution for every current or operation point.

## 2.5. Computation of the Optimal $g_m/I_D$

As pointed out in the previous section, the 1:1 capacitive matching condition at the input of the front-end amplifier holds in the global optimum. Therefore, replacing $C_{gs} = C_K$ in (2.3) does not change the optimal solution of the minimization problem. Consequently, $I_D(x)$ can be expressed as:

$$I_D(x) = \frac{I_D}{C_{gs}}(x) \cdot C_K. \tag{2.6}$$

Using (2.6) in (2.3) and eliminating the constant terms, the minimization problem to solve becomes

$$\text{MIN}_x \ \frac{\int_0^\infty |H(j\omega)|^2 \cdot N(x,\omega)\,\mathrm{d}\omega}{\frac{I_D}{C_{gs}}(x)}. \tag{2.7}$$

By taking the derivative of (2.7) with respect to $x$ and equating to zero, the condition for the optimal value of the input device operation point $x^*$, for which the *ENC*$^2$ is

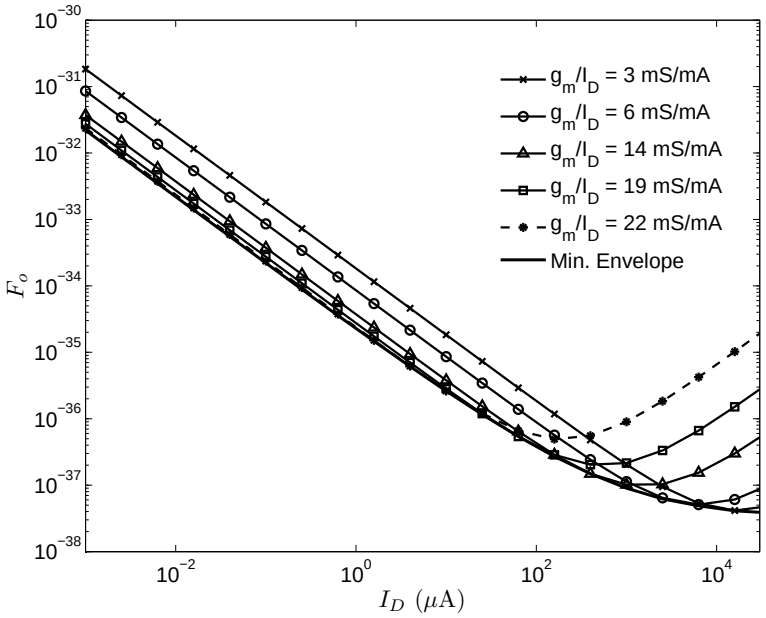



FIGURE 2.5. $F_o$ as a function of $I_D$ for different operation points and $K_F = 0$. The input device optimal operation point is at $x^* = 1.48$ mS/mA.

minimum, can be determined:

$$\frac{\frac{I_D}{C_{gs}}'(x^*)}{\frac{I_D}{C_{gs}}(x^*)} = \frac{\int_0^\infty |H(j\omega)|^2 \cdot N'(x^*,\omega)\,\mathrm{d}\omega}{\int_0^\infty |H(j\omega)|^2 \cdot N(x^*,\omega)\,\mathrm{d}\omega}. \tag{2.8}$$

In Fig. 2.7, left and right terms of (2.8) are shown for the same conditions of Fig. 2.4, where the intersection point of the curves, which represents the optimal value $x^*$, is pointed out. Although this condition allows to find $x^*$ with an error of $3.6\%$ compared to the solution found graphically in Fig. 2.4, it requires generating look-up tables for noise considering a particular filter transfer function, which is impractical for its use in a design-oriented methodology.

Given that

$$\frac{I_D}{C_{gs}}(x) = \frac{1}{x} \cdot \frac{g_m}{C_{gs}}(x) \tag{2.9}$$

the left term of (2.8) can be expressed as:

$$\frac{\frac{I_D}{C_{gs}}'(x)}{\frac{I_D}{C_{gs}}(x)} = \frac{\omega_T'(x)}{\omega_T(x)} - \frac{1}{x} \tag{2.10}$$

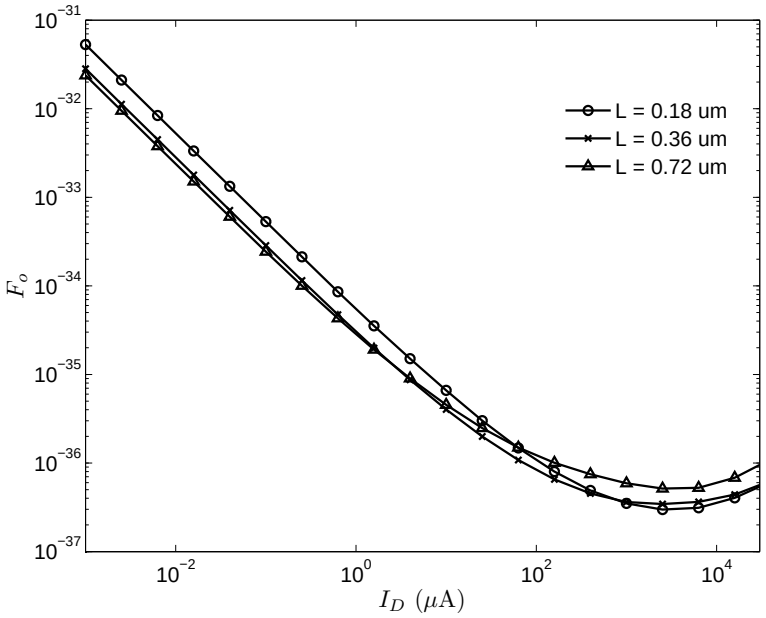



FIGURE 2.6. Minimum envelope of $F_o$ as a function of $I_D$ for different length values.

where $\omega_T(x)$ is the input device transit frequency (defined as $g_m/C_{gs}$). To simplify the right term of (2.8), a modified expression of $N(x,\omega)$ is necessary. Without loss of generality, the flicker noise component dependency on the frequency can be assumed to be $1/\omega^{A_F}$, where $A_F$ is the flicker noise coefficient. Thus, $N(x,\omega)$ can be written as:

$$N(x,\omega) = W(x) + F(x) \cdot \frac{1}{\omega^{A_F}} \tag{2.11}$$

where $W(x)$ is the white noise contribution and $F(x)/\omega^{A_F}$ is the $1/f$ noise contribution. Both $W(x)$ and $F(x)$ are constant for a given operation point, and they are related to each other through the corner frequency $\omega_c(x)$:

$$F(x) = \omega_c(x)^{A_F} W(x). \tag{2.12}$$

Considering the above simplifications, $N(x,\omega)$ can be finally expressed as:

$$N(x,\omega) = W\left(x\right)\left(1 + \left(\frac{\omega_c\left(x\right)}{\omega}\right)^{A_F}\right) \tag{2.13}$$

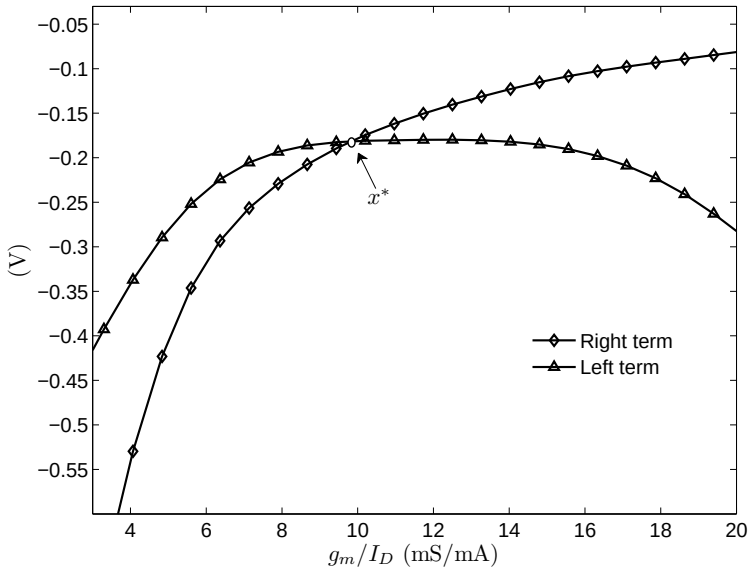



FIGURE 2.7. Both terms of (2.8). The intersection point, which represents the input device optimal operation point, is at $x^* = 9.83$ mS/mA.

and its derivative can be expressed as:

$$\begin{aligned} N'(x,\omega) &= W'(x)\left(1+\left(\frac{\omega_c(x)}{\omega}\right)^{A_F}\right) \\ &\quad + W(x)\,\frac{A_F\cdot\omega_c'(x)\cdot\omega_c(x)^{A_F-1}}{\omega^{A_F}}. \end{aligned} \tag{2.14}$$

Furthermore, the normalization $t = t'/\tau_p$ can be applied on the filter pulse response. This allows to work with tables of filter coefficients that depend only on the pulse shape, thus, the condition to find $x^*$ can be expressed as

$$\frac{\omega_T'(x^*)}{\omega_T(x^*)} - \frac{1}{x^*} = \frac{W'(x^*)}{W(x^*)} + \frac{A_F\cdot\omega_c'(x^*)\cdot\omega_c(x^*)^{A_F-1}}{\frac{a_w}{\tau_p^{A_F}a_f(A_F)} + \omega_c(x^*)^{A_F}} \tag{2.15}$$

where $a_w$ is the white noise coefficient and $a_f(A_F)$ is the flicker noise coefficient (De Geronimo & O'Connor, 2005). These coefficients can be computed as

$$a_w = \frac{1}{2\pi\left|\max\left[g\left(t'/\tau_p\right)\right]\right|^2}\int_0^\infty |H(jy)|^2\ \mathrm{d}y \tag{2.16}$$

$$a_f(A_F) = \frac{1}{2\pi \left|\max\left[g\left(t'/\tau_p\right)\right]\right|^2} \int_0^\infty \frac{\left|H(jy)\right|^2}{y^{A_F}}\, \mathrm{d}y \tag{2.17}$$

where $y = \tau_p \omega$.

Assuming $W(x) \propto x^{-1}$ (evident from the thermal noise models of Table 2.1) and $A_F \approx 1$, for strong inversion operation, the expression in (2.15) can be further simplified to:

$$\frac{\omega_T'(x^*)}{\omega_T(x^*)} = \frac{\omega_c'(x^*)}{\frac{a_w}{\tau_p a_f} + \omega_c(x^*)}. \tag{2.18}$$

Finally, assuming $W(x) \propto x^{-2}$ (see Table 2.1) and $A_F \approx 1$, for weak inversion operation, the expression in (2.15) can be further simplified to:

$$\frac{\omega_T'(x^*)}{\omega_T(x^*)} = -\frac{1}{x^*} + \frac{\omega_c'(x^*)}{\frac{a_w}{\tau_p a_f} + \omega_c(x^*)}. \tag{2.19}$$

The conditions shown in (2.18) and (2.19) establish the lower ($x_s^*$, for strong inversion operation) and upper ($x_w^*$, for weak inversion operation) limits of $x^*$, respectively. Then $x^*$ can be computed as the weighted average of $x_s^*$ and $x_w^*$. The weight of each factor depends on how dominant the flicker noise is. High values of $\omega_c$ move the v-shaped curves to the left of the $F_o$ vs. $I_D$ plot (see Fig. 2.4), reaching high values of $x^*$ – weak inversion operation –, meanwhile low values of $\omega_c$ move the v-shaped curves to the right of the $F_o$ vs. $I_D$ plot, reaching low values of $x^*$ – strong inversion operation –.

In Fig. 2.8 both terms of (2.18) and (2.19) are shown for the same conditions of Fig. 2.4. The intersection points of the curves, which represent $x_s^*$ and $x_w^*$, are pointed out. The optimal operation point, $x^*$, lays in between these boundaries. For simplicity in this specific case, considering that the value of $x^*$ obtained from Fig. 2.4 suggests operation close to strong inversion, $x_s^*$ could be used as an initial estimation with an additional advantage: filter and noise data are obtained independently, the first one from normalized filter tables and the second one from normalized noise power curves as functions of $x$. It is worth mentioning that the data must be carefully manipulated, since (2.8), (2.18) and (2.19) are sensitive to numerical approximations.

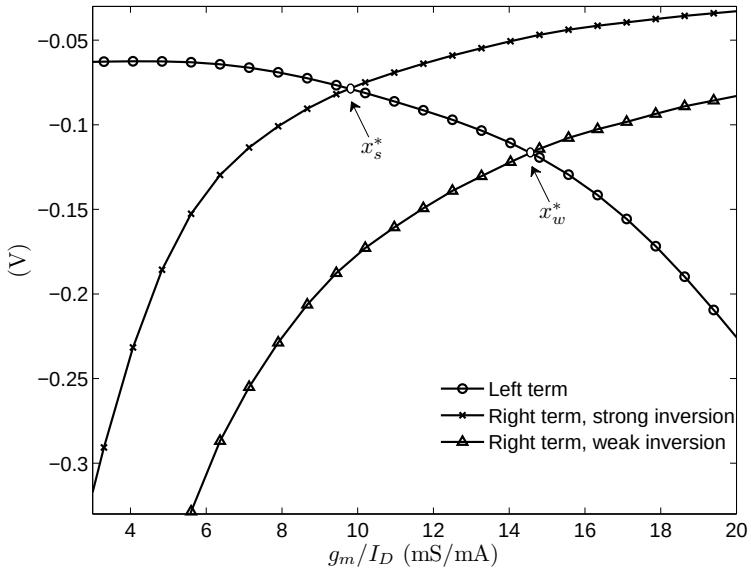



FIGURE 2.8. Left term of (2.18) and (2.19), and both right terms. The intersection points, which represent the input device optimal operation point for each operation region, are $x_s^* = 9.78$ mS/mA and $x_w^* = 14.5$ mS/mA.

Typical values of $a_w/a_f$ are between $1.3$ and $2.3$ (De Geronimo & O'Connor, 2005), thus the denominator of (2.18) can be simplified to $\approx 2/\tau_p + \omega_c(x^*)$ since $\tau_p$ is the responsible for the order of magnitude of the factor $a_w/\tau_p a_f$. In this particular case, the result obtained for $x^*$ does not change significantly ($x^* = 9.98$ mS/mA for $a_w/a_f = 1.3$ and $x^* = 9.29$ mS/mA for $a_w/a_f = 2.3$). In case the noise specifications to meet are not too stringent, an additional simplification can be tolerated and an approximate surround of the optimal operation point of the front-end input device can be determined solely by using the pulse peaking time of the filter and ignoring the pulse shape. Additionally, it can be observed that flicker noise, which is responsible of the non monotonicity of the noise for high currents, is related to the pulse peaking time magnitude as follows: lower values of $\tau_p$ in (2.18) imply lower values of $x^*$, which are related to high values of $\omega_c$. Therefore, when $\tau_p$ decreases, flicker noise contribution increases.

Finally, the conditions expressed in (2.18) and (2.19) reveal that the existence of a noise minimum is related to the sensitivity of $\omega_T$ with respect to $x$, and somehow to the sensitivity of $\omega_c$ with respect to $x$.

## 2.6. Conclusion

This chapter shows a different view on a widely studied problem, noise optimization for particle physics electronics. The approach followed is based on an extension of the $g_m/I_D$ methodology to allow noise analysis.

The results found show that, although capacitance matching represents the minimum noise for constant $g_m/I_D$, it is not a Pareto-optimal solution for low noise and low power circuits, where the power budget is limited; instead, lower capacitance and a different operation point is preferred. It is also shown that the device length optimization requires further study, because minimum length does not necessarily provide the optimal solution.

This chapter also presents an analysis on the dependence of the noise limit (assuming infinite power available) on flicker noise, and shows a method that allows to compute the operation point and current for which minimum noise is achieved, based only on technology data and filter parameters. This methodology provides a new insight on the impact of flicker noise in electronic systems for radiation detection. This work evidences that flicker noise is related with the existence of a finite current for which noise is minimum, and also outlines the relation between flicker noise and the filter peaking time.

# 3. A 10-BIT SAR ADC WITH CONFIGURABLE INL

In particle physics experiments, the instrumentation circuit of a typical detector includes a detector, an amplifier, a filter, a buffer, an ADC, and a readout circuit. This chapter deals with the design of the 10-bit successive approximation register (SAR) analog-to-digital converter (ADC) with configurable integral non-linearity (INL), which is meant to be used in the front-end electronics integrated circuit for the BeamCal detector. The converter features a power-saving state and a configurable INL, which allows to correct the non-linearity of the circuits connected to the ADC.

## 3.1. Introduction

As explained previously in Chapter 1, a typical particle physics experiment detector system contains different layers of detectors, each of which is usually highly segmented into a multichannel array. Each channel includes a detector, an amplifier (whose noise analysis was covered in Chapter 2), a filter, a buffer, an ADC, and a readout circuit (Abusleme, 2011; Spieler, 2005). For the analog-to-digital conversion, the use of a 10-bit fully-differential successive SAR ADC with a sampling rate of 3.25MS/s is proposed (Abusleme, 2011; Abusleme et al., 2012; McCreary & Gray, 1975), which is a good candidate for the digitalization due to circuit simplicity, small footprint and low power consumption.

In this chapter, the design of a 10-bit SAR ADC with configurable INL is presented. Fig. 3.1 shows a simplified diagram of the 10-bit SAR ADC, where $D_{out}$ is the serial digital output signal and $v_{in}$ is the differential input voltage to be converted. The clock signals have been omitted from this figure. The ADC comprises a charge-redistribution switched-capacitor digital-to-analog converter (DAC) network, the SAR logic and a voltage comparator preceded by an amplifier that reduces offset, noise and possible metastability problems. All digital circuits in the ADC are based on standard CMOS logic gates.

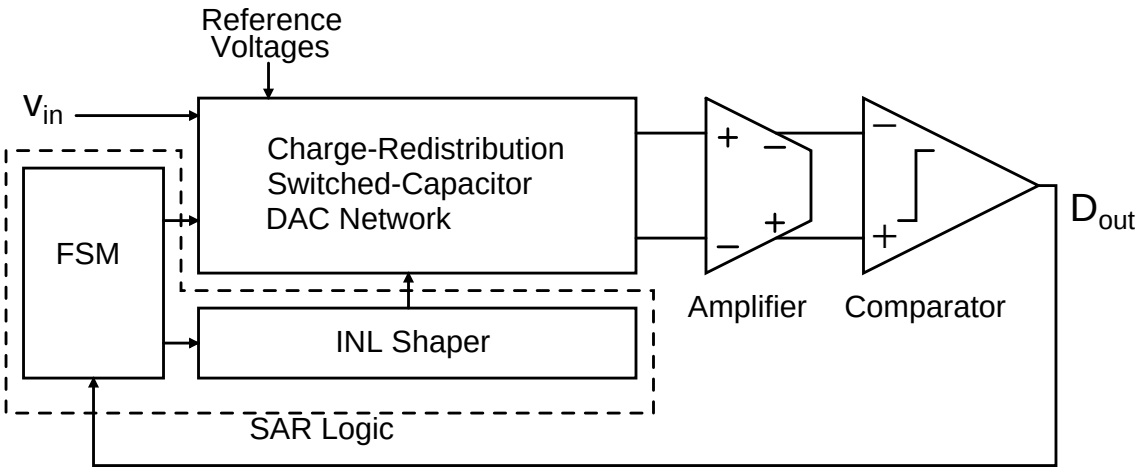



FIGURE 3.1. SAR ADC block diagram.

The SAR ADC amplifier and comparator were designed to operate on a locally-generated, non-overlapping two-phase clock.

As it will be explained later, the DAC capacitor array is divided into two sections: a binary-weighted one and a thermometer-coded one. Since the thermometer-coded capacitor array improves the ADC DNL, smaller capacitors can be used, which reduces the converter input capacitance and power consumption. The capacitors, implemented through a parallel connection of unit capacitors scattered over a $32 \times 32$ array, are subject to radial effects, so the ADC non-linearity is dependent on the order in which these capacitors are connected during the conversion process. As shown in Fig. 3.1, the SAR logic is composed by a finite state machine (FSM) and a block called INL shaper. The FSM consists of a sequential circuit and is responsible for setting the DAC input upon the comparator output, so the DAC output successively converges to the differential input value. The INL shaper consists of a combinational circuit that defines the order in which the DAC array capacitors are connected throughout a conversion, so the ADC INL can be manipulated and used to correct or cancel out the non-linearities of other circuits connected to the ADC, such as the charge-sense amplifier (CSA).

In the following sections, the operation of the SAR ADC is explained.

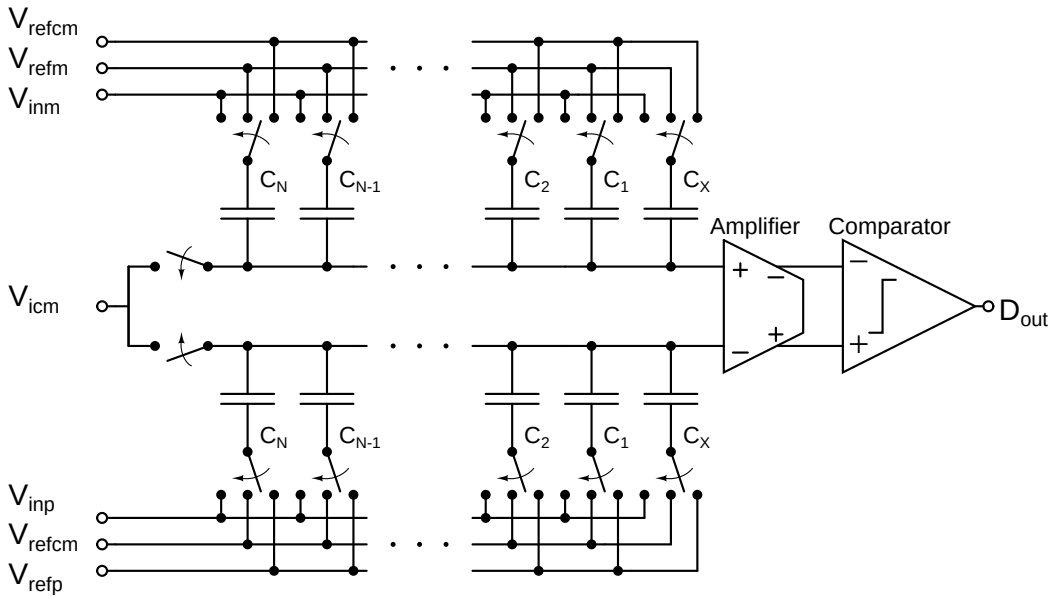



FIGURE 3.2. Charge-redistribution switched-capacitor DAC network, preamplifier and comparator.

### 3.2. Successive Approximation Register and DAC Array

A generic diagram of the charge-redistribution switched-capacitor DAC network, omitting the SAR logic, is depicted in Fig. 3.2, where $N$ is the number of bits, $V_{refcm}$, $V_{refm}$, $V_{refp}$ and $V_{icm}$ are the reference voltages, and $V_{inp}$ and $V_{inm}$ are the analog input signals. As shown in the figure, two DAC switched-capacitor arrays are used.

There are $N+2$ subcycles per conversion. Since each converted bit requires one subcycle, there is a 2-subcycle overhead for reset. During reset, the amplifier inputs are connected to $V_{icm}$ to set the amplifier's initial common-mode input voltage, and the capacitor arrays are switched to $V_{inp}$ and $V_{inm}$, sampling the differential input voltage. After the reset period, the common-mode switches are opened and the capacitor arrays are connected to the negative references, $V_{refcm}$ for the bottom half circuit and $V_{refm}$ for the top half circuit. At this time, the amplifier differential input becomes $(V_{inp}-V_{inm})-(V_{refcm}-V_{refm})$. Then, on each bit test, from MSB ($i=N$) to LSB ($i=1$), the corresponding capacitors are connected to the positive references, $V_{refp}$ for the bottom half circuit and $V_{refcm}$ for the top half

circuit. Since the capacitors are binary-weighted, with $C_i = 2^{i-1} \cdot C_X$, on bit test $i$ the amplifier differential input decreases by $V_{FSR}/2^{N-i+1}$, where $V_{FSR} = V_{refp} + V_{refm} - 2 \cdot V_{refcm}$ is the differential input full-scale range. The successive approximation register sets the DAC input based upon the comparator output, and the DAC output thus successively converges to the ADC differential input value.

Although the capacitor array is nominally binary-weighted, different implementation techniques can be used. These techniques cover different regions in the design space, trading capacitance spread[1] and area, linearity, input capacitance and circuit complexity. For example, a series capacitor in the array produces a split or segmented array, which presents a reduced input capacitance, area and capacitor spread, but makes the array linearity sensitive to parasitic capacitances to ground (Chen & Brodersen, 2006). Calibration is then usually necessary to meet linearity specifications. A thermometer-coded array offers a reduced ADC differential non-linearity (DNL), at the cost of additional logic for a binary-to-thermometer decoder (Kuttner, 2002). The spread in capacitor values is reduced, whereas the area and input capacitance are unchanged. The decoder size increases exponentially with the number of bits in the binary output. Thus, a practical solution is to thermometer-encode only the five most significant bits, as shown in Fig. 3.3.

In order to reduce the ADC input capacitance and area, small capacitors are used, and two different capacitor structures were considered: metal-insulator-metal (MIM) capacitors and metal-oxide-metal (MOM) capacitors such as the ones shown in (Abusleme et al., 2012). In the $180$-nm process used, MIM capacitors are made of parallel plates on metal 5 and CAPM (single MIM top plate metal), with a capacitance of 1 fF/$\mu$m$^2$ and a minimum size limited by design rules. Lateral-field MOM capacitors are made of closely-placed metal layers. Compact MOM capacitor cells with adequate capacitor-to-capacitor shielding can be achieved with a custom design. In this context, the capacitance lower limit is set by matching constraints, as opposed to design rules, and a lower input capacitance than with MIM capacitors can be achieved.

[1]The capacitance spread is defined as the ratio between the maximum capacitance and the minimum capacitance.

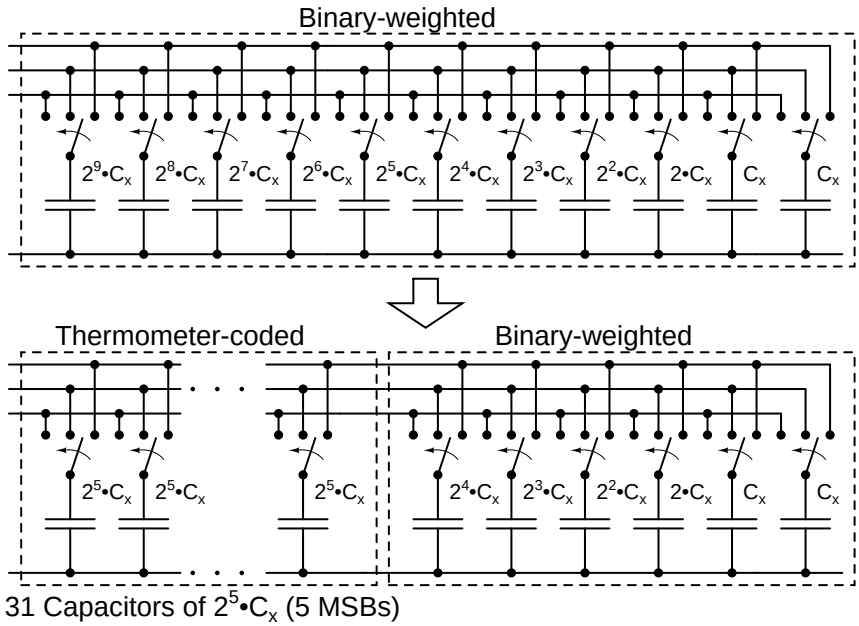



FIGURE 3.3. Thermometer-coded capacitors array.

MOM capacitors were designed with a target unit capacitance of 2 fF per metal layer, or a total array capacitance close to 2 pF. A three-dimensional view of the MOM capacitor designed is shown in Fig. 3.4, and a three-dimensional view of an array of MOM capacitors is shown in Fig. 3.5. Another array with two layers and twice the capacitance was also designed. The metal structure capacitance was extracted using Space 3D layout-to-circuit extractor software from Delft University (Van Genderen & Van der Meijs, 2000). The capacitor arrays were also shielded with a top and bottom plate of metal connected to ground, in order to isolate them from the rest of the circuit. This shield adds capacitance to ground, which does not affect de circuit linearity but attenuates the pre-amplifier input voltage. The top shielding layer has been omitted from Fig. 3.4 and Fig. 3.5.

### 3.3. Amplifier

Fig. 3.6 shows the ADC pre-amplifier, which corresponds to a fully-differential amplifier with active PMOS load, a polarization branch and a passive common-mode feedback

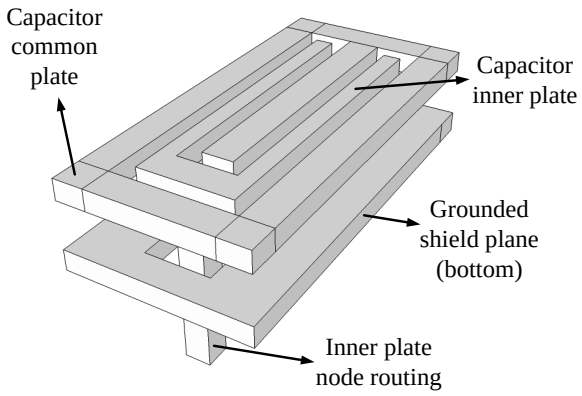



FIGURE 3.4. Three-dimensional view of the $2.52\mu$m$\times 6.375\mu$m MOM capacitor designed with top shielding layer omitted. The capacitor common plate corresponds to the terminal connected to the amplifier input (see Fig. 3.2).

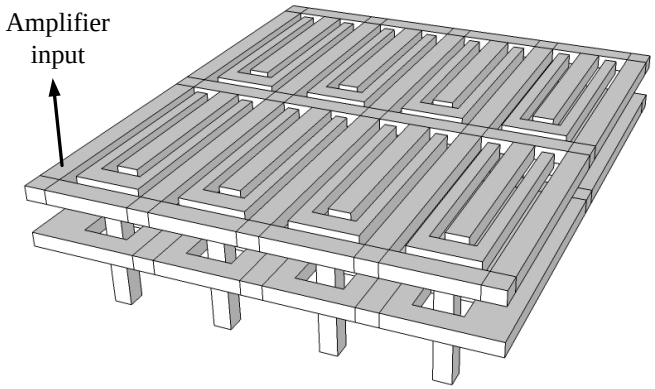



FIGURE 3.5. Three-dimensional view of an array of MOM capacitors with top shielding layer omitted.

(CMFB) circuit (Feldman et al., 1998) implemented with CMOS switches and four capacitors. Transistors $M_{in1}$ and $M_{in2}$ are the input devices, $M_{c1}$ and $M_{c2}$ are the active loads, $M_T$ is the preamplifier bias current source, voltages $v_{ip}$ and $v_{im}$ are the input signals, $v_{op}$ and $v_{om}$ are the output signals, and $V_{ocm}$ is the desired output common-mode voltage. The amplifier device sizes are shown in Table 3.1.

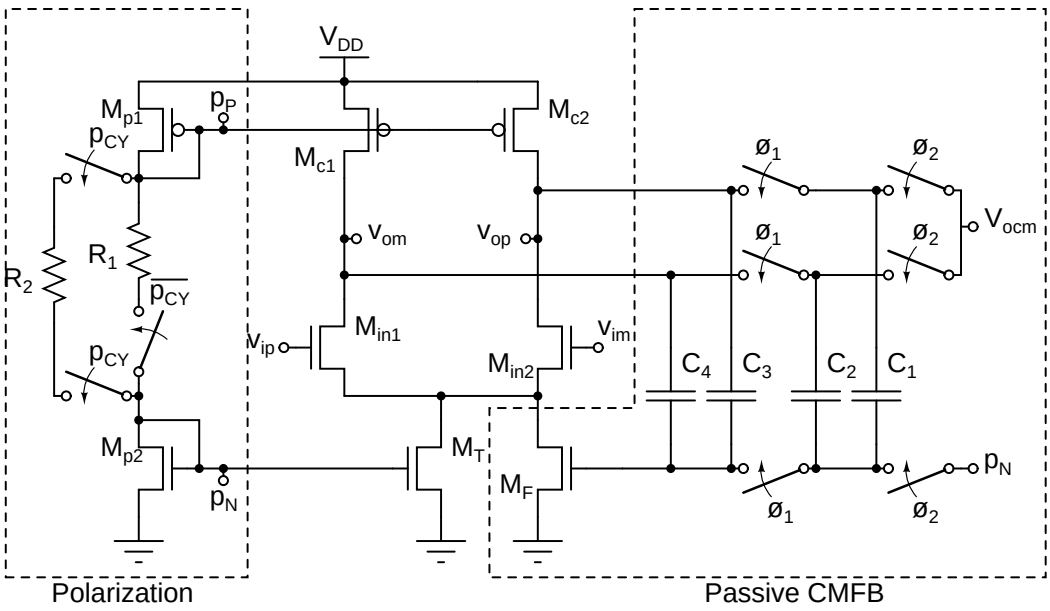



FIGURE 3.6. Amplifier schematic, including the passive CMFB loop.

TABLE 3.1. Amplifier device sizes.

| Transistor | $L$ [$\mu$m] | $W$ [$\mu$m] | Value |
|---|---|---|---|
| $M_T$ | 0.18 | 17.14 | — |
| $M_F$ | 0.18 | 7.34 | — |
| $M_{in1}$ and $M_{in2}$ | 0.18 | 12.24 | — |
| $M_{c1}$ and $M_{c2}$ | 0.18 | 10.08 | — |
| $M_{p1}$ | 0.18 | 2.52 | — |
| $M_{p2}$ | 0.18 | 4.285 | — |
| $C_1$ and $C_2$ | — | — | 20 fF |
| $C_3$ and $C_4$ | — | — | 40 fF |
| $R_1$ | — | — | 7 k$\Omega$ |
| $R_2$ | — | — | 80 k$\Omega$ |

Given that the ADC clock frequency is 52 MHz (3.25MS/s), and that the amplifier has a period of $\approx$ 20 ns to settle its output, its cut-off frequency was initially determined in order to have six time constants in half a period, that is $f_c = 95$ MHz. The noise constraint was set so that the amplifier input-referred noise voltage is equal to half of the quantization noise power $N_q$, which is given by

$$N_q = \frac{LSB^2}{12} \tag{3.1}$$

where $LSB = V_{FSR}/2^B$, $B = 10$, and $V_{FSR}$ was assumed to be equal to 1 V.

The amplifier parameters shown in Table 3.1 were chosen in order to maximize its gain considering the constraints detailed above, and an arbitrary maximum current per branch of $100$ $\mu$A. By using the $g_m/I_D$ technique (Silveira et al., 1996; Flandre et al., 1997), the design space was swept completely and the amplifier gain, cut-off frequency and input-referred noise voltage were evaluated for each point in the design space until an optimal solution was found.

Since the ADC is meant to be used as a part of a system with a low duty cycle of $0.5\%$, the amplifier features a low-power operation state, which is controlled by the power-cycling signal $p_{CY}$. This signal controls the current of the polarization branch, and hence sets the current of all the amplifier branches. When $p_{CY}$ is low, the current source of the polarization branch is determined by $R_1$, whereas when $p_{CY}$ is high, this current is determined by $R_2$. As shown in Table 3.1 $R_2 > R_1$, so $p_{CY}$ high implies smaller currents in the circuit.

### 3.4. Comparator

The ADC comparator, shown in Fig. 3.7, corresponds to the conventional latched comparator shown in (Miyahara & Matsuzawa, 2009; Jeon & Kim, 2010), which is the result of several contributions made in the latch-type comparators field (Wicht et al., 2004; Schinkel et al., 2007; Jeon & Kim, 2010). The comparator device sizes are shown in Table 3.2.

The comparator has two phases of operation. During the reset phase ($\phi$ input low), $M_{T1}$ is closed, $M_{r1}$ and $M_{r2}$ pull node voltages $D_m$ and $D_p$ to $V_{DD}$, turning off transistors $M_{T2}$ and $M_{T3}$, and transistors $M_{ri}$ ($i = 3-6$) pull the remaining node voltages to ground. During the compare phase ($\phi$ input high), the positive feedback through transistors $M_{ci}$ ($i = 1 - 4$) swings the output nodes toward different rails, according to the differential input on $M_{in1}$ and $M_{in2}$. The differential input voltage $v_{ip} - v_{im}$ determines the currents through transistors $M_{in1}$ and $M_{in2}$, which discharge the capacitances to ground at nodes

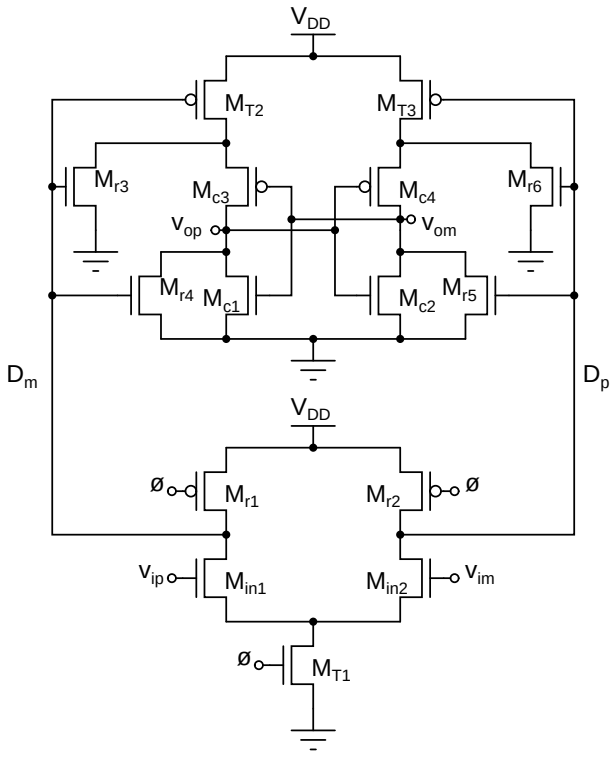



FIGURE 3.7. Double-tail dynamic latched comparator.

$D_m$ and $D_p$. For example, let us suppose that $v_{ip} > v_{im}$. Therefore, node $D_m$ will be discharged faster than node $D_p$, gradually turning on transistor $M_{T2}$ before $M_{T3}$ and gradually turning off transistors $M_{r3}$ and $M_{r4}$ before $M_{r5}$ and $M_{r6}$. As the reset transistors $M_{ri}$ ($i = 3 - 6$) turn off and the tail transistors $M_{Ti}$ ($i = 2 - 3$) turn on, the inverters composed by $M_{c1}$-$M_{c3}$ and $M_{c2}$-$M_{c4}$ try to pull their respective outputs to $V_{DD}$, but since $M_{r3}$, $M_{r4}$ and $M_{T2}$ switch state faster than $M_{r5}$, $M_{r6}$ and $M_{T3}$, $v_{op}$ is finally pulled to $V_{DD}$, forcing $v_{om}$ to ground.

The offset analysis for similar comparator topologies has been widely studied in the literature (Jeon et al., 2011; Nikoozadeh & Murmann, 2006), and some dynamic offset compensation techniques has been proposed (Miyahara & Matsuzawa, 2009; Miyahara et al., 2008), but since the comparator offset, which is already attenuated by the amplifier gain, only introduces a global offset in the transfer characteristics of the conventional SAR ADC presented here, there is no need to use any of these techniques.

TABLE 3.2. Comparator device sizes.

| Transistor | $L$ [$\mu$m] | $W$ [$\mu$m] |
|---|---|---|
| $M_{T1}$ | 0.18 | 11.52 |
| $M_{T2}$ and $M_{T3}$ | 0.18 | 4.32 |
| $M_{in1}$ and $M_{in2}$ | 0.18 | 5.76 |
| $M_{r1}$ and $M_{r2}$ | 0.18 | 17.28 |
| $M_{r3}$, $M_{r4}$, $M_{r5}$ and $M_{r6}$ | 0.18 | 2.88 |
| $M_{c1}$ and $M_{c2}$ | 0.18 | 1.44 |
| $M_{c3}$ and $M_{c4}$ | 0.18 | 4.32 |

## 3.5. INL shaper

As explained previously, the converter capacitor array comprises a binary-weighted section for the five LSBs and a thermometer-coded section for the five MSBs (see Fig. 3.3). Fig. 3.8 shows the distribution of the capacitors in the layout. All capacitors were implemented through a parallel connection of unit capacitors, and scattered over the $32 \times 32$ array on a common-centroid fashion. Capacitors $C_1$ to $C_5$ are the binary-weighted capacitors, whereas capacitors $T_1$ to $T_{31}$ are the thermometer-coded capacitors.

Depending on the fabrication process, there are different reasons why there could be radial effects on a wafer. For instance, chemical-mechanical planarization/polishing (CMP) is a process of smoothing and planarizing surfaces with the combination of chemical reactions and mechanical forces, and is the preferred planarization step utilized in deep sub-micron IC manufacturing (Zhengfeng et al., 2001). During the CMP of wafers, copper dishing[2] leads to deviations from the ideal case producing a radial effect that alters, in this case, the capacitors capacitance. The radial effect makes the capacitors closest to the array edges larger, and the capacitors at the array center smaller, so the order in which the capacitors are connected alters the ADC linearity. For instance, the capacitors can be connected in a way that minimizes the ADC sensitivity to radial gradients, improving its linearity. Moreover, the ADC non-linearity can be leveraged to cancel out the non-linearity of another stage of the system in which the ADC is being used (Abusleme et al., 2012).

[2]Copper dishing is defined as the difference in height between the lowest and highest point of the dish.

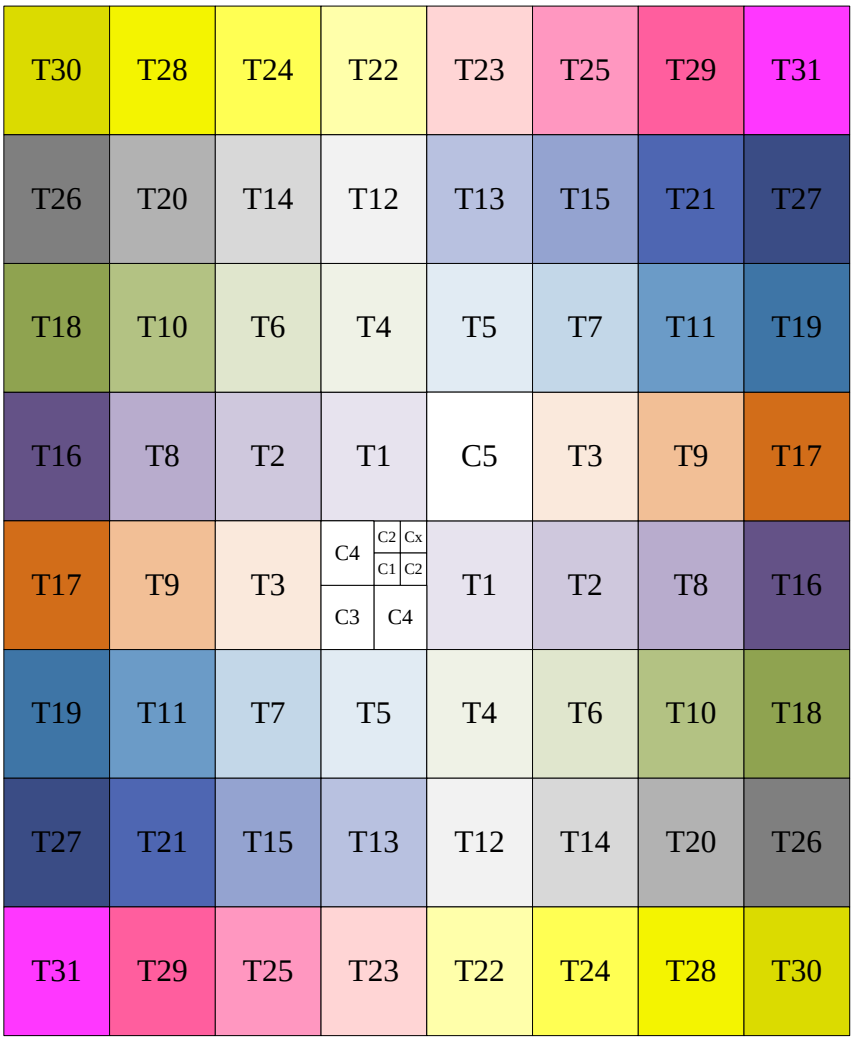


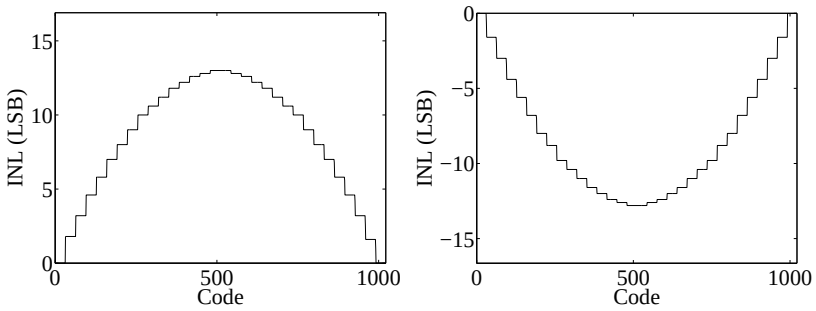

FIGURE 3.8. Capacitors distribution in the layout. Capacitors $C_1$ to $C_5$ are binary-weighted, and capacitors $T_1$ to $T_{31}$ are thermometer-coded. Notice the common centroid technique.

Considering the dimensions of the unit capacitor and the distribution shown in Fig. 3.8, it can be determined which capacitors will be larger and which capacitors will be smaller after the fabrication by computing the distance from every capacitor to the center of the array. The capacitance deviation of the capacitor increases with this distance. Table 3.3 shows the DAC array capacitors sorted from the smallest to the largest for the MOM capacitors and MIM capacitors used.

TABLE 3.3. DAC array capacitors from the smallest to the largest.

| | MOM ($2.52\mu$m×$6.375\mu$m) | MIM ($3.5\mu$m×$6.375\mu$m) |
|---|---|---|
| $C_{s1}$ | $T_1$ | $T_1$ |
| $C_{s2}$-$C_{s3}$ | $T_2$-$T_3$ | $T_2$-$T_3$ |
| $C_{s4}$-$C_{s5}$ | $T_8$-$T_9$ | $T_8$-$T_9$ |
| $C_{s6}$-$C_{s7}$ | $T_{16}$-$T_{17}$ | $T_4$-$T_5$ |
| $C_{s8}$-$C_{s9}$ | $T_4$-$T_5$ | $T_6$-$T_7$ |
| $C_{s10}$-$C_{s11}$ | $T_6$-$T_7$ | $T_{16}$-$T_{17}$ |
| $C_{s12}$-$C_{s13}$ | $T_{10}$-$T_{11}$ | $T_{10}$-$T_{11}$ |
| $C_{s14}$-$C_{s15}$ | $T_{18}$-$T_{19}$ | $T_{18}$-$T_{19}$ |
| $C_{s16}$-$C_{s17}$ | $T_{12}$-$T_{13}$ | $T_{12}$-$T_{13}$ |
| $C_{s18}$-$C_{s19}$ | $T_{14}$-$T_{15}$ | $T_{14}$-$T_{15}$ |
| $C_{s20}$-$C_{s21}$ | $T_{20}$-$T_{21}$ | $T_{20}$-$T_{21}$ |
| $C_{s22}$-$C_{s23}$ | $T_{26}$-$T_{27}$ | $T_{26}$-$T_{27}$ |
| $C_{s24}$-$C_{s25}$ | $T_{22}$-$T_{23}$ | $T_{22}$-$T_{23}$ |
| $C_{s26}$-$C_{s27}$ | $T_{24}$-$T_{25}$ | $T_{24}$-$T_{25}$ |
| $C_{s28}$-$C_{s29}$ | $T_{28}$-$T_{29}$ | $T_{28}$-$T_{29}$ |
| $C_{s30}$-$C_{s31}$ | $T_{30}$-$T_{31}$ | $T_{30}$-$T_{31}$ |

As mentioned earlier, the INL of the ADC can be manipulated by changing the order in which the thermometer-coded capacitors are connected during a conversion. The INL shaper, which is basically a multiplexer with a two-bit selector $Sel$, 31 input bits and 31 output bits, allows four different capacitors distributions, which generate four different INLs. Fig. 3.9 shows four different INLs extracted from behavioral simulations. In order to generate the INL shown in Fig. 3.9(a), the array capacitors should be connected from the smallest to the largest (from $C_{s1}$ to $C_{s31}$). If the capacitors are connected backwards (i.e., from $C_{s31}$ to $C_{s1}$), the INL from Fig. 3.9(b) should be obtained. In order to generate the INL shown in Fig. 3.9(c), the array capacitors should be connected alternating the larger capacitors with the smaller capacitors as follows $C_{s1}$, $C_{s31}$, $C_{s2}$, $C_{s30}$, ... $C_{s17}$, $C_{s16}$. If the capacitors are connected backwards, the INL from Fig. 3.9(d) should be obtained.




(a) $Sel = 00$. (b) $Sel = 01$.

(c) $Sel = 10$. (d) $Sel = 11$.

FIGURE 3.9. Simulated ADC non-linearity resulting from different INL shaper inputs.

## 3.6. Conclusion

A fully-differential successive approximation ADC with configurable INL has been presented. The converter comprises two DAC capacitor arrays, each one of them composed by a thermometer-coded array and a binary-weighted array, a voltage comparator, an amplifier to attenuate the comparator noise and offset voltage, an INL shaper to change the order in which the DAC array capacitors are connected during the conversion, and a finite state machine. For the DAC capacitor arrays, customized MOM capacitors were designed in order to reduce the input capacitance and power consumption. The converter features a power-saving state and a configurable INL, which allows to compensate the non-linearity of the circuits connected to the ADC taking advantage of the otherwise detrimental radial effects.

# 4. PASSIVE REFERENCE-SHARING SAR ADC

Charge-redistribution successive approximation register (SAR) analog-to-digital converters (ADCs) are widely used for their simple architecture, inherent low-power consumption and small footprint. Several techniques aiming to reduce the power consumption, to increase the speed, and to reduce the capacitance spread have been developed, such as splitting the digital-to-analog converter (DAC) capacitor array, and charging and discharging the DAC capacitors in multiple steps. In this chapter, a fully-differential, low-power, passive reference voltage sharing SAR ADC architecture is presented along with its noise and non-idealities analysis and simulation results. This architecture can be implemented using small capacitors, since the reference voltage is scaled down by successively connecting equally-sized capacitors in parallel. Therefore, the capacitors minimum size is limited by either the unit capacitance mismatch or by noise considerations.

## 4.1. Introduction

SAR ADCs have gained significant popularity since the introduction of the charge redistribution analog-to-digital conversion techniques (McCreary & Gray, 1975). This widespread use is mainly due to their inherent low-power consumption, small footprint and simple architecture, which make them suitable for low-power, medium-resolution applications such as wireless networks and medical monitoring (Yip & Chandrakasan, 2011; Scott et al., 2003). In the recent years, several techniques to reduce the power consumption, to reduce the capacitance spread, and to increase the sample rate of SAR-based ADC architectures have been developed, such as splitting the DAC capacitor array (Yee et al., 1979), charging and discharging the DAC capacitors in multiple steps (Van Elzakker et al., 2008), using a comparator-based asynchronous binary-search technique (CABS) (Van der Plas & Verbruggen, 2008), programming the comparator threshold at runtime to approximate the input signal via binary search (Nuzzo et al., 2009), and carrying out the successive approximation algorithm by means of a passive charge-sharing (PCS) process (Craninckx

& Van der Plas, 2007). Nowadays, medium-resolution (8 to 10 bits) SAR ADCs have achieved sampling rates of tens of MS/s with power consumptions of only tens of fJ per conversion-step (C.-C. Liu et al., 2010; Scott et al., 2003; Shikata et al., 2011; Tsai et al., 2011; Yip & Chandrakasan, 2011; Van Elzakker et al., 2008; Craninckx & Van der Plas, 2007).

To perform the successive approximation algorithm in the fully-differential PCS architecture introduced in (Craninckx & Van der Plas, 2007), binary-weighted capacitors pre-charged with the reference voltage are successively connected to the comparator input. This way, the converter operates in the charge domain without the need of a buffered active reference. However, unlike conventional SAR ADCs, this architecture has its resolution limited because its linearity is sensitive to the comparator offset (Imani & Bakhtiar, 2008). In any case, the PCS process has proven to be an effective technique to achieve a reduction in the power consumption.

In all SAR ADCs reported in the literature a considerable fraction of the die area is occupied by the DAC capacitor array (Yip & Chandrakasan, 2011; Scott et al., 2003; Van Elzakker et al., 2008; Van der Plas & Verbruggen, 2008; Nuzzo et al., 2009; C.-C. Liu et al., 2010; Shikata et al., 2011; Tsai et al., 2011; Imani & Bakhtiar, 2008; Craninckx & Van der Plas, 2007), and the large capacitance is a limiting factor when trying to reduce the power consumption (Shikata et al., 2011) and increase the conversion rate. In this chapter, a fully-differential, passive reference-sharing (PRS) SAR ADC based on the PCS ADC of (Craninckx & Van der Plas, 2007) is presented, which allows the use of small, equally-sized capacitors. Additionally, an analysis is presented in order to determine both the sensitivity of the PRS architecture to variations of different parameters and the factors that limit its resolution. Simulation results are also presented.

## 4.2. The Passive Reference-Sharing Algorithm

To perform the successive approximation algorithm in the PCS ADC (Craninckx & Van der Plas, 2007), an array of binary-weighted capacitors is charged with a reference

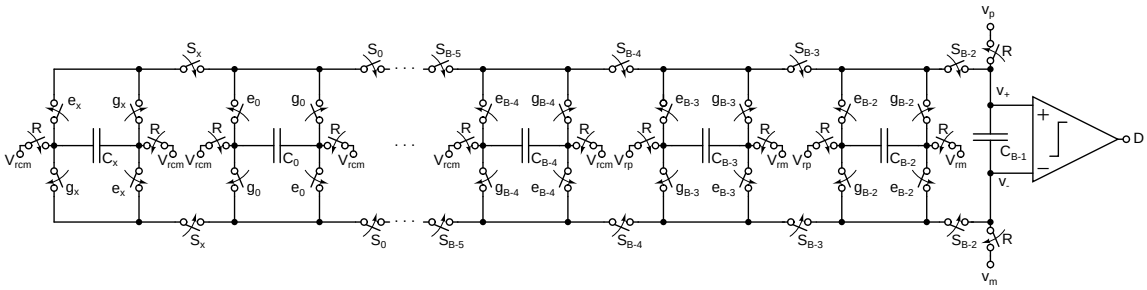



FIGURE 4.1. Simplified schematic of a $B$-bit passive reference-sharing SAR ADC.

voltage while the analog signal is sampled. Then, based upon the previous decision of the comparator, the next capacitor is connected to the comparator input in such a way that the comparator differential input voltage converges to zero as the conversion progresses. The comparator decisions that lead to this result represent the ADC digital output, from MSB to LSB. The PCS process itself can also be used to scale the reference voltage at the terminals of each capacitor in a binary progression, so that the DAC capacitors can be sized equally and the chip area can be reduced considerably.

The PRS algorithm consists of two processes that occur in parallel: the reference-sharing (RS) and the successive approximation (SA) process. While the analog signal is sampled, only two capacitors are charged with the differential reference voltage. Then, as the SA process progresses, the capacitors that are still unconnected to the comparator input successively share their reference charge with the remaining uncharged capacitors. At every step of the RS process the charge of one capacitor is shared with another capacitor with the same capacitance, hence its charge is split in equal parts and the voltage at its terminals is halved. Through this process, the initial reference charge is propagated through the array, so the reference voltages at the terminals of the capacitors end up scaled in a binary progression.

Fig. 4.1 shows a simplified schematic of a $B$-bit PRS ADC, where all capacitors are sized equally, voltages $v_p$ and $v_m$ are the input signals, and $V_{rp}$, $V_{rm}$ and $V_{rcm}$ are the reference voltages. Fig. 4.2 illustrates the step-by-step operation of a $4$-bit PRS ADC. Considering $v_{id} = v_p - v_m$ and $V_{ref} = 2\,(V_{rp} - V_{rm})$, the converter works as follows: at

the track-and-hold step (step 0), only the reset signal $R$ is high, so $C_{B-1}$ is charged to $v_{id}$, $C_{B-2}$ and $C_{B-3}$ are charged to $V_{ref}/2$ and the remaining capacitors are short-circuited to $V_{rcm}$. At the first conversion step (step 1), $R$ turns low and the MSB ($D_1$) is determined. Signals $S_{B-4}$, $e_{B-3}$ and $e_{B-4}$ turn high and $C_{B-3}$ shares its charge with $C_{B-4}$, leaving a voltage of $V_{ref}/4$ at both capacitors. At the $i$-th step (for $i \geq 2$), $S_{B-i}$ turns high and $C_{B-i}$, holding a reference voltage of $V_{ref}/2^{i-1}$, is connected either directly or inversely between nodes $v_+$ and $v_-$ (signal $e_{B-i}$ turns high if $D_{i-1} = 0$, or signal $g_{B-i}$ turns high if $D_{i-1} = 1$). At the same step, $S_{B-(i+2)}$ turns low, signals $S_{B-(i+3)}$ and $e_{B-(i+3)}$ turn high and $C_{B-(i+2)}$ shares its charge with $C_{B-(i+3)}$, leaving a voltage of $V_{ref}/2^{i+1}$ at both capacitors. This process continues until the LSB ($D_B$) is determined, after which the state machine returns to step 0. Capacitor $C_x$ is never connected between nodes $v_+$ and $v_-$, since its only function is to halve the reference voltage at $C_0$.

The maximum clock rate for this architecture is limited by the on resistance $r_{on}$ of the switches and the DAC array capacitance. In turn, the minimum value of $r_{on}$ is limited by the maximum size of the switches. Larger switches imply larger parasitic capacitances, which degrade the charge-sharing process due to the capacitive voltage divider composed by the array capacitances and the gate-to-source/drain capacitances of the transistors.

Neglecting the parasitic capacitances and assuming perfect matching between the capacitors of the array, the comparator differential input voltage at the $i$-th step of the conversion $v_{in}^{PRS}(i) = v_{PRS}(i) + V_{OS}$ can be computed as (4.1). For the PCS ADC (Craninckx & Van der Plas, 2007), $v_{in}^{PCS}(i) = v_{PCS}(i) + V_{OS}$ can be computed as (4.2). In both equations, $V_{OS}$ represents the input-referred comparator offset voltage.

$$v_{in}^{PRS}(i) = \frac{1}{i}\left(v_{id} \pm \frac{V_{ref}}{2} \pm \frac{V_{ref}}{4} \cdots \pm \frac{V_{ref}}{2^{i-1}}\right) + V_{OS} \tag{4.1}$$

$$v_{in}^{PCS}(i) = \frac{1}{2 - \frac{2}{2^i}}\left(v_{id} \pm \frac{V_{ref}}{2} \pm \frac{V_{ref}}{4} \pm \cdots \pm \frac{V_{ref}}{2^{i-1}}\right) + V_{OS}. \tag{4.2}$$

Equations (4.1) and (4.2) reveal the main drawback of these architectures, which is their sensitivity to $V_{OS}$. As pointed out in (Imani & Bakhtiar, 2008), the linearity of

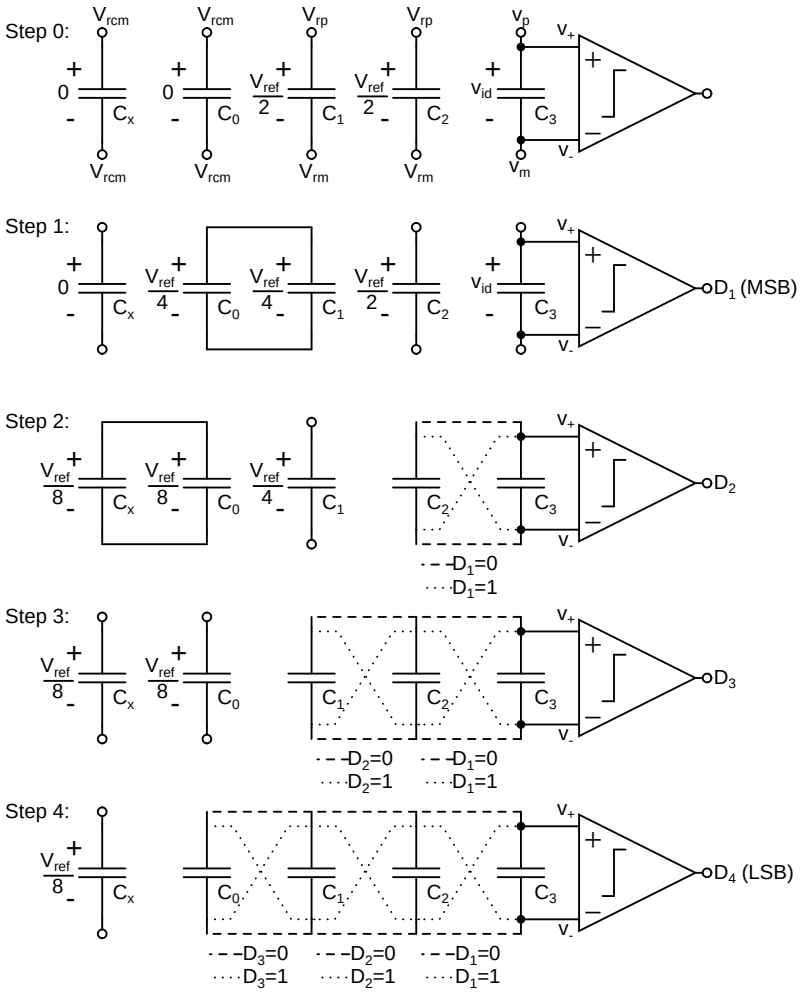



FIGURE 4.2. Illustration of the step-by-step operation of a $B = 4$-bit passive reference-sharing SAR ADC.

PCS-based ADCs is sensitive to $V_{OS}$, whereas in an ordinary SAR architecture this voltage only introduces an offset in the ADC transfer characteristics. It can be seen that $V_{OS}/v_{PCS}(i)$ doubles after a few conversion steps, whereas $V_{OS}/v_{PRS}(i)$ increases proportionally with the conversion step. This limits the maximum resolution achievable by the PRS ADC, unless offset calibration techniques are implemented.

The energy consumed by the PRS ADC from the reference power supply $E_{ref}^{PRS}$ can be computed as (4.3), whereas $E_{ref}^{PCS}$ can be computed as (4.4). In both equations, $C_{tot}$

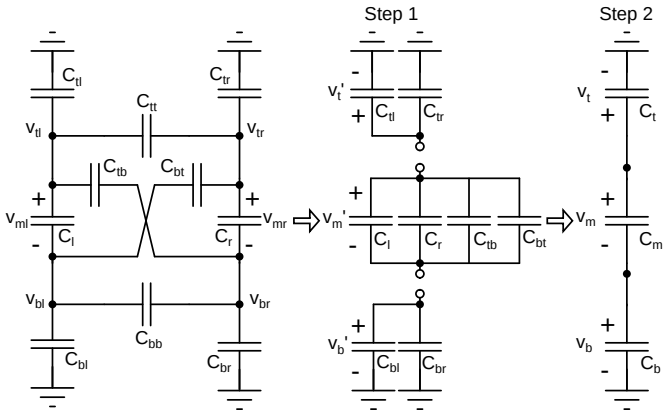



FIGURE 4.3. Circuit schematic for parasitic capacitances analysis.

represents the total capacitance of the DAC capacitor array.

$$E_{ref}^{PRS} = \frac{1}{4\left(B+1\right)} C_{tot} V_{ref}^2 \tag{4.3}$$

$$E_{ref}^{PCS} = \frac{1}{2} C_{tot} V_{ref}^2. \tag{4.4}$$

For a given $C_{tot}$, $E_{ref}^{PRS}$ is lower than $E_{ref}^{PCS}$ by a factor of $2\left(B+1\right)$. Additionally, considering that $C_{tot}^{PRS} = \left(B+1\right)C$ and $C_{tot}^{PCS} = \left(2^B-1\right)C$, where $C$ represents the smallest capacitance of the capacitor array, and without taking into account the consumption of the digital circuits and the comparator consumption, the energy consumed by the PRS ADC does not depend on the number of bits $B$, and it is lower than that of the PCS ADC by a factor of $2\left(2^B-1\right)$.

## 4.3. Non-Idealities due to Parasitic Capacitances

The circuit schematic for the parasitic capacitances analysis is depicted in Fig. 4.3. Subscript $t$ stands for top, $b$ for bottom, $m$ for middle, $l$ for left, and $r$ for right. Therefore, $C_r$ is the capacitor connected to the comparator input, $C_{tr}$ and $C_{br}$ represent the top and bottom parasitic capacitances to ground at nodes $v_{tr}$ and $v_{br}$, respectively, $C_l$ is the next capacitor to be connected to the comparator input, and $C_{tl}$ and $C_{bl}$ represent its parasitic capacitances to ground from top and bottom terminals. Capacitors $C_{tt}$, $C_{tb}$, $C_{bt}$ and $C_{bb}$,

namely parasitic cross capacitances, model the parasitic capacitances due to factors that depend on the layout.

When connecting $C_l$ and $C_r$ directly ($tl$ to $tr$ and $bl$ to $br$), $C_{tt}$ and $C_{bb}$ are short-circuited and capacitances $C_{tb}$ and $C_{bt}$ are added to the total capacitance at the comparator input ($C_m$ in Fig. 4.3). When connecting $C_l$ and $C_r$ inversely ($tl$ to $br$ and $bl$ to $tr$), $C_{tb}$ and $C_{bt}$ are short-circuited and capacitances $C_{tt}$ and $C_{bb}$ are added to $C_m$. As shown in Fig. 4.3, the analysis can be split into two steps. Assuming that $C_l$ and $C_r$ are connected directly, the first step consists of connecting, separately, capacitors $C_{tl}$ and $C_{tr}$, capacitors $C_l$, $C_r$, $C_{tb}$ and $C_{bt}$, and capacitors $C_{bl}$ and $C_{br}$. Thus, $C_t$, $C_m$ and $C_b$ can be readily computed as

$$C_t = C_{tl} + C_{tr} \tag{4.5}$$

$$C_m = C_l + C_r + C_{tb} + C_{bt} \tag{4.6}$$

$$C_b = C_{bl} + C_{br} \tag{4.7}$$

and voltages $v_t^{'}$, $v_m^{'}$ and $v_b^{'}$ can be computed as

$$v_t^{'} = \frac{C_{tl}v_{tl} + C_{tr}v_{tr}}{C_t} \tag{4.8}$$

$$v_m^{'} = \frac{C_l v_{ml} + C_r v_{mr} + C_{tb}v_{tl,br} + C_{bt}v_{tr,bl}}{C_m} \tag{4.9}$$

$$v_b^{'} = \frac{C_{bl}v_{bl} + C_{br}v_{br}}{C_b} \tag{4.10}$$

where $v_{a,b} \triangleq v_a - v_b$. In the second step, $C_t$, $C_m$ and $C_b$ are connected and the node voltages can be computed according to the excess voltage of the previous step $\Delta = v_b^{'} + v_m^{'} - v_t^{'}$ and the effect of the capacitor voltage divider of the resulting circuit on $\Delta$ as

follows

$$v_t = v_t^{'} + \Delta \frac{C_m||C_b}{C_m||C_b + C_t} \tag{4.11}$$

$$v_m = v_m^{'} - \Delta \frac{C_t||C_b}{C_t||C_b + C_m} \tag{4.12}$$

$$v_b = v_b^{'} - \Delta \frac{C_m||C_t}{C_m||C_t + C_b} \tag{4.13}$$

where $x||y \triangleq xy/(x+y)$. In order to compute the node voltages when the comparator decision leads to an inverse connection of $C_l$ and $C_r$, subscripts $tl$ and $bl$ must be swapped, and $C_{tt}$ and $C_{bb}$ must be used instead of $C_{bt}$ and $C_{tb}$.

Taking into account that the capacitance of each individual capacitor of the array is $C$, let us assume that parasitic capacitances to ground of each capacitor are symmetrical and can be modeled as $\alpha C$; and parasitic cross capacitances are equal and can be modeled as $\gamma C$. Considering these assumptions, $C_r$ and $C_{tr}$ (equal to $C_{br}$) at the $i$-th step of the conversion (for $i \geq 2$) can be expressed as

$$C_r = C(i-1) + 2\gamma C(i-2) \tag{4.14}$$

$$C_{tr} = \alpha C(i-1) \tag{4.15}$$

and the results shown in (4.11)-(4.13) along with the excess voltage $\Delta$ can be written as

$$\Delta = v_{ml}\left(\frac{1+\gamma}{i+2\gamma(i-1)} - \frac{1}{i}\right) + v_{mr}\left(\frac{1}{i} - \frac{1+3\gamma}{i+2\gamma(i-1)}\right) \tag{4.16}$$

$$v_t = \frac{1}{i}v_{tl} + \left(1 - \frac{1}{i}\right)v_{tr} + \Delta \frac{1}{2 + \frac{i\alpha}{i+2\gamma(i-1)}} \tag{4.17}$$

$$v_m = v_{ml}\left(\frac{1+\gamma}{i+2\gamma(i-1)}\right) + v_{mr}\left(1 - \frac{1+3\gamma}{i+2\gamma(i-1)}\right) - \Delta \frac{1}{1 + \frac{2i+4\gamma(i-1)}{i\alpha}} \tag{4.18}$$

$$v_b = \frac{1}{i}v_{bl} + \left(1 - \frac{1}{i}\right)v_{br} - \Delta \frac{1}{2 + \frac{i\alpha}{i+2\gamma(i-1)}}. \tag{4.19}$$

To compute the node voltages when connecting $C_l$ and $C_r$ inversely, subscripts $tl$ and $bl$ must be swapped and $v_{ml}$ must be replaced by $-v_{ml}$.

Assuming $\alpha = 0$ and $\gamma = 0$, the results shown in (4.16)-(4.19) can be further simplified to

$$\Delta^{ideal} = 0 \tag{4.20}$$

$$v_t^{ideal} = \frac{1}{i} v_{tl} + \left(1 - \frac{1}{i}\right) v_{tr} \tag{4.21}$$

$$v_m^{ideal} = \frac{1}{i} v_{ml} + \left(1 - \frac{1}{i}\right) v_{mr} \tag{4.22}$$

$$v_b^{ideal} = \frac{1}{i} v_{bl} + \left(1 - \frac{1}{i}\right) v_{br}. \tag{4.23}$$

Based on the comparison between (4.16)-(4.19) and (4.20)-(4.23), several conclusions can be drawn. As seen in (4.16), $\Delta$ is a non-ideality produced by the parasitic cross capacitances when the parasitic capacitances to ground are symmetrical. Moreover, symmetrical parasitic capacitances to ground do not affect the ideal performance of the circuit when $\gamma \approx 0$. Also, large parasitic capacitances to ground ($\alpha \gg \gamma$) help to mitigate the effect of $\gamma$ without affecting the converter performance. Behavioral simulations results using (4.16)-(4.19) show that, when increasing $\gamma$ for a fixed value of $\alpha$, the end-point codes are susceptible to move out of the full-scale input range. Therefore the parasitic cross capacitances effect results in a resolution reduction, since there are fewer codes to represent the whole input voltage range.

## 4.4. Noise Analysis

Given that the operation of the PRS ADC requires a large number of switching steps, the contribution of the $kT/C$ noise poses a limit on the resolution of this architecture. After the track-and-hold step, each capacitor holds a voltage noise power of $kT/C$. Then the RS process makes the capacitors share their initial noise contributions, adding another $kT/C$ contribution to every capacitor that shares its charge. At the end of the RS process, each capacitor holds the effects of fractions of different noise processes, which are correlated to fractions of the noise held by other capacitors in the array. Let us call $(kT/C)_i$ the total integrated noise at the capacitor $C_i$ after the track-and-hold step, and $(kT/C)_{i,i-1}$

the noise contribution added to capacitors $C_i$ and $C_{i-1}$ after $C_i$ shares its charge to $C_{i-1}$. Then, after the RS process finishes, the total integrated noise $N_{C_i}$ at each capacitor (see Fig. 4.1) can be computed as

$$N_{C_{B-1}} = \left(\frac{kT}{C}\right)_{B-1} \tag{4.24}$$

$$N_{C_{B-2}} = \left(\frac{kT}{C}\right)_{B-2} \tag{4.25}$$

$$N_{C_{B-3}} = \frac{1}{2}\left(\frac{kT}{C}\right)_{B-3} + \frac{1}{2}\left(\frac{kT}{C}\right)_{B-4} + \left(\frac{kT}{C}\right)_{B-3,B-4} \tag{4.26}$$

$$N_{C_{B-4}} = \frac{1}{2}N_{C_{B-3}} + \frac{1}{2}\left(\frac{kT}{C}\right)_{B-5} + \left(\frac{kT}{C}\right)_{B-4,B-5} \tag{4.27}$$

and so on. For the worst-case scenario, and considering that $kT/C$ contributions with the same subscript are correlated and must be added as signals, the input-referred noise as a function of the number of bits $N(B)$ can be computed as

$$N(B) = B^2 \cdot \sum_{i=0}^{B-1} N_{C_i} \tag{4.28}$$

where factor $B^2$ is due to the attenuation of the signal at the comparator input evidenced in (4.1). Since the complexity of (4.28) makes it non suitable for design, $N(B)$ can be approximated to

$$N(B) = \begin{cases} B^2 \cdot 2^{B-1}\dfrac{kT}{C} & B \leq 6; \quad \text{(4.29a)} \\ B^2 \cdot B^2\dfrac{kT}{C} & \text{otherwise.} \quad \text{(4.29b)} \end{cases}$$

Fig. 4.4 shows the exact $kT/C$ factors of (4.28) along with the $kT/C$ factors of (4.29a) and (4.29b) as a function of $B$. Equation (4.29a) is within $\pm 15\%$ of (4.28), whereas (4.29b) overestimates (4.28) by $14\%$, approximately.

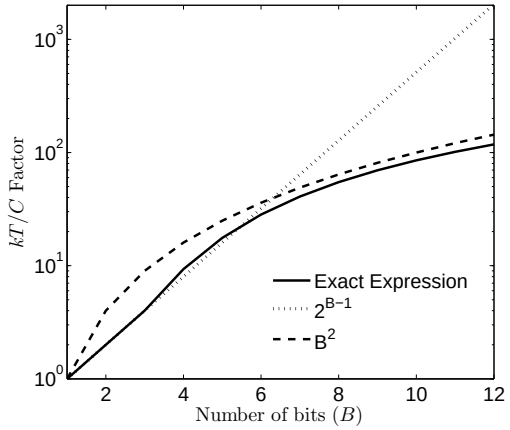



FIGURE 4.4. $kT/C$ noise factors as a function of the number of bits $B$.

For instance, for a $B$-bit converter in a 0.18-$\mu$m technology, using $V_{ref} = 1.8$ V and omitting mismatch considerations, the minimum value of $C$ could be determined according to the design consideration $N(B) \leq (LSB/2)^2$, which leads to $C \geq 6$ fF for $B = 6$, and to $C \geq 200$ fF for $B = 7$, both results calculated for $T = 300$ K.

## 4.5. Other Considerations

Other design aspects of the PRS ADC have also been analyzed, such as the input common-mode voltage effects on the ADC performance, the minimum capacitance, charge injection effects of the switches, and the control signals timing considerations. Each one of these topics is detailed below.

### 4.5.1. Input Common-Mode Voltage $V_{ccm}$

To avoid fluctuations of $V_{ccm}$ throughout a conversion, which may affect the comparator performance, parasitic capacitances to ground must be well matched. Since $V_{ccm}$ is sensitive to the relative difference between the parasitic capacitances, large values of $\alpha$ help to mitigate this problem without degrading the converter performance. Assuming perfect matching between the parasitic capacitances to ground and neglecting the cross

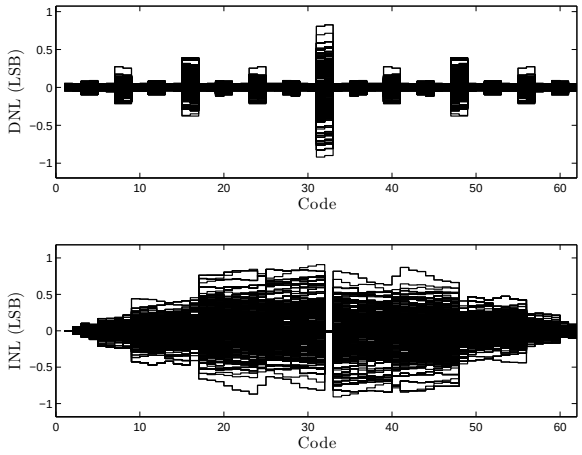



FIGURE 4.5. Simulated DNL and INL of a 6-bit PRS ADC for $1000$ realizations and a unit capacitance mismatch of $\sigma = 1.31\%$.

capacitances, $V_{ccm}$ at the $i$-th step of the conversion can be expressed as

$$V_{ccm}(i) = \left(1 - 2^{-i}\right) V_{rcm} + 2^{-i} v_{icm} \tag{4.30}$$

so the signal input common-mode voltage $v_{icm}$ and the reference common-mode voltage $V_{rcm}$ should be equal in order to reduce the fluctuations of $V_{ccm}$.

### 4.5.2. Minimum Capacitance

The DAC capacitors minimum size is limited either by process mismatch considerations, by the sensitivity of the ADC transfer characteristics to systematic cross capacitances, or by noise considerations. When the resolution is low enough so that noise constrains can be neglected, the process mismatch should be considered to compute the capacitors minimum size, which can be determined through Monte Carlo behavioral simulations using the Pelgrom mismatch coefficients (Pelgrom et al., 1989). To determine the effects of the cross capacitances, behavioral simulations shall be used. Fig. 4.5 shows the simulated DNL and INL of a 6-bit PRS ADC considering a unit capacitance mismatch of $\sigma = 1.31\%$. A total of $1000$ simulations were run, producing a yield of $99.6\%$[1]. It can be observed that the mid-range code INL is 0 in all simulations due to the symmetrical characteristics of this converter architecture.

[1]Only $0.4\%$ of the realizations presented missing codes.

### 4.5.3. Charge Injection

During the RS process, when a switch opens, it injects charge that alters the common-mode reference voltage $V_{refcm}$ and the differential reference voltage $V_{refdif}$ (Sheu et al., 1987). Assuming that charges $Q_t$ and $Q_b$ are injected at the top node and bottom node of capacitor $C$, respectively, and assuming symmetrical parasitic capacitances to ground equal to $\alpha C$, $V_{refcm}$ and $V_{refdif}$ can be computed as

$$V_{refcm} = V_{refcm}^{ideal} + \frac{1}{\alpha C}\frac{(Q_t + Q_b)}{2} \tag{4.31}$$

$$V_{refdif} = V_{refdif}^{ideal} + \frac{1}{(2+\alpha)\,C}(Q_t - Q_b) \tag{4.32}$$

where $V_{refcm}^{ideal} = V_{rcm}$ and $V_{refdif}^{ideal} = V_{ref}/2,\ V_{ref}/4,\ V_{ref}/8$, and so on. Large values of $\alpha$ help to mitigate the effects of the charge injection. CMOS switches shall be used to reduce $Q_t$ and $Q_b$, and bootstrap techniques can be used to reduce $|Q_t - Q_b|$. Also, in order to reduce $Q_t$ and $Q_b$, smaller switches shall be used, resulting in an increase of the dominant time constant and compromising the ADC maximum sampling rate.

### 4.5.4. Timing Considerations

In ordinary SAR ADCs the charge in the input nodes of the comparator does not change during the conversion, whereas in PCS-based SAR ADCs, the charge changes at every step of the conversion and it is not possible to pull back a decision. Because of this, some of the control signals of the PRS ADC must be handled carefully (see Fig. 4.1):

- in order to avoid short circuits between $V_{rcm}$, $V_{rp}$ ,$V_{rm}$, $v_p$ and $v_m$, control signals $S_i$ ($\forall i$) and $R$ should be non-overlapped;
- when sharing the reference voltage, control signals $S_{B-i}$ and $S_{B-(i+1)}$ ($\forall i \geq 4$) should be non-overlapped; and
- in order to avoid the unwanted discharge of the capacitors, control signals $e_i$ and $g_i$ ($\forall i$) should be non-overlapped.

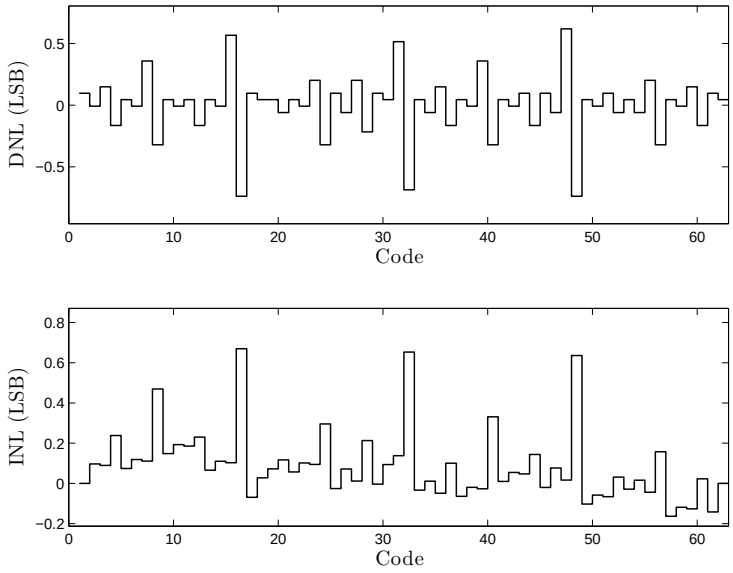



FIGURE 4.6. Simulated DNL and INL of a 6-bit PRS ADC using SPICE.

## 4.6. Simulation Results

A 6-bit PRS ADC was designed for a $0.18$-$\mu$m technology using minimum-size CMOS switches, fully-symmetrical $100$-fF capacitors and the conventional comparator topology of (Miyahara & Matsuzawa, 2009)[2]. Simulations were carried out using SPICE, where parasitic capacitances to ground of 20 fF were considered. To test the circuit, an input ramp on $v_{id}$ from $-1.8$ V to $1.8$ V was used, the reference voltages were set at $V_{rp} = 1.35$ V, $V_{rm} = 0.45$ V and $V_{rcm} = 0.9$ V, and the clock frequency was set at $f = 2$ MHz. Fig. 4.6 shows the DNL and INL obtained from the simulation. It can be observed that the mid-range code INL is 0, as mentioned in the previous section.

## 4.7. Conclusion

A fully-differential passive reference-sharing SAR ADC technique has been presented, along with its noise and non-idealities analysis and simulations. The converter features a capacitance spread of one, a small area, a low-power consumption and a reconfigurable resolution. The detailed analysis shows that, in order to design a practical circuit, the

[2]Generic 0.18-$\mu$m transistor models available at MOSIS website (*MOSIS*, 2013) were used for this work.

parasitic capacitors to ground must be well matched, the cross parasitic capacitances between adjacent capacitors in the array must be minimized, and that both the comparator input-referred offset and the $kT/C$ noise limit the converter resolution.

# 5. TEST RESULTS

Three versions of the 10-bit SAR ADC introduced in Chapter 3 and the PRS ADC introduced in Chapter 4 were design and implemented in a $0.18$ $\mu$m technology. The SAR ADC was implemented using 2-fF MOM capacitors, 4-fF MOM capacitors and 5-fF MIM capacitors. The converters were placed in a 7.8 mm$^2$ die, fabricated and characterized for static performance metrics.

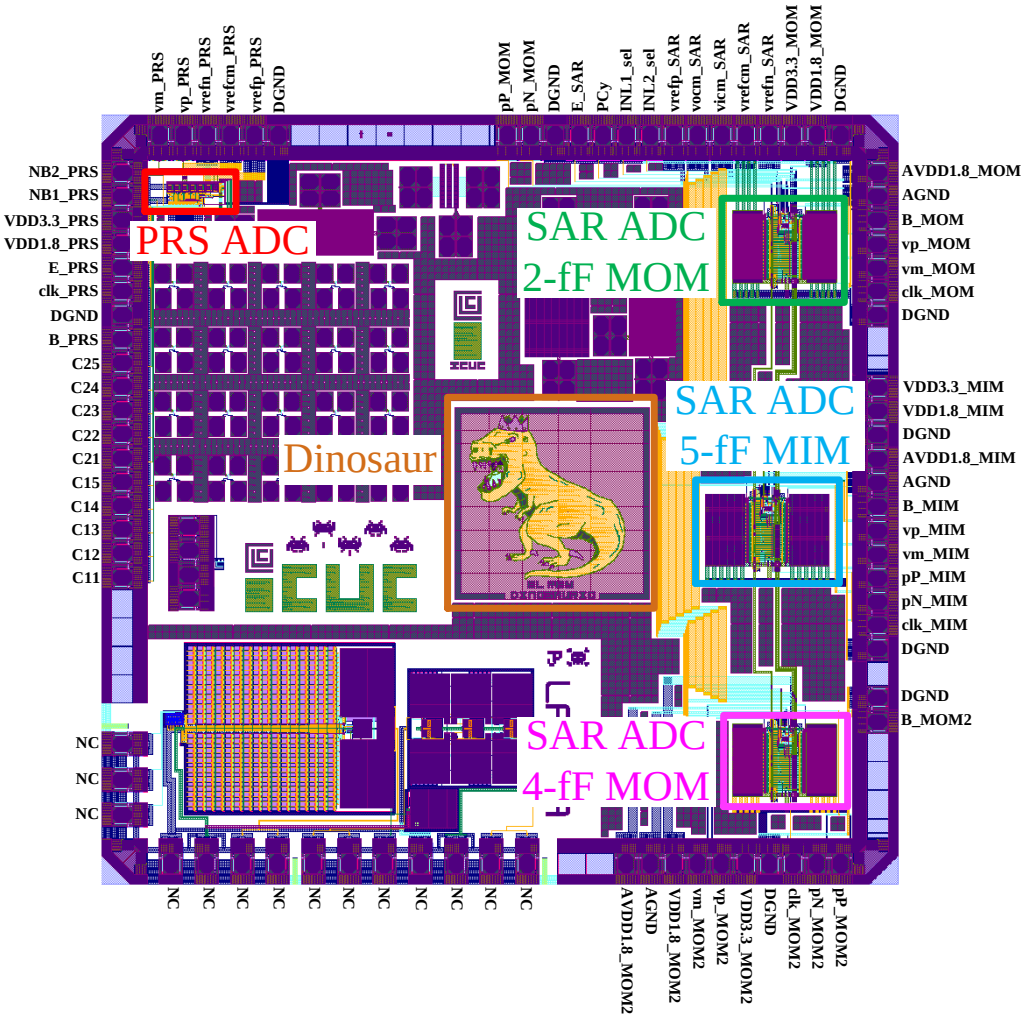



FIGURE 5.1. Prufpilo, dimensions: 2.742mm$\times$2.84 mm = 7.8 mm$^2$.

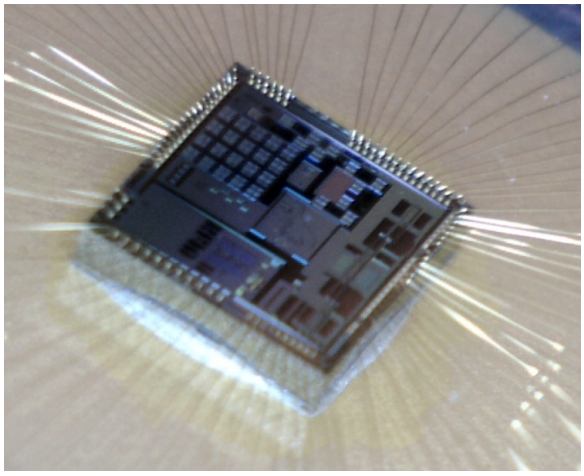


FIGURE 5.2. Prufpilo IC micrograph.

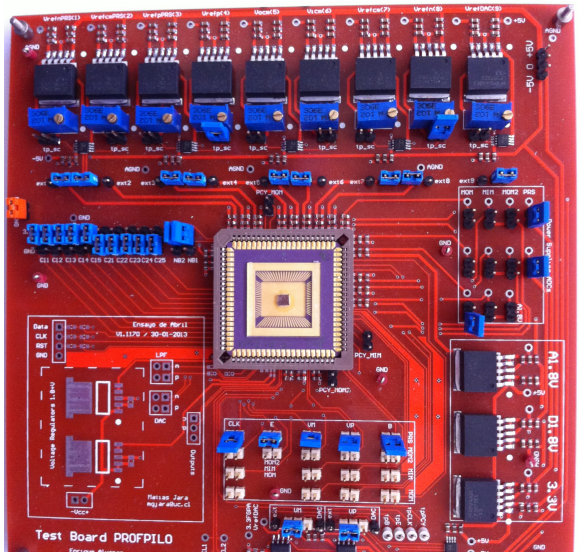



FIGURE 5.3. Prufpilo test board.

Fig 5.1 shows the layout of the 84-pad IC fabricated (hereafter, Prufpilo), where the converters position in the die and the pads names are indicated. For a detailed description of the IC pinout, see Appendix A. Fig 5.2 shows a die micrograph of Prufpilo, and Fig 5.3 shows the custom printed circuit board used for the tests. The test board consists of several reference voltages and two 16-bit DACs controlled externally by an FPGA to generate the analog input signals for the ADCs.

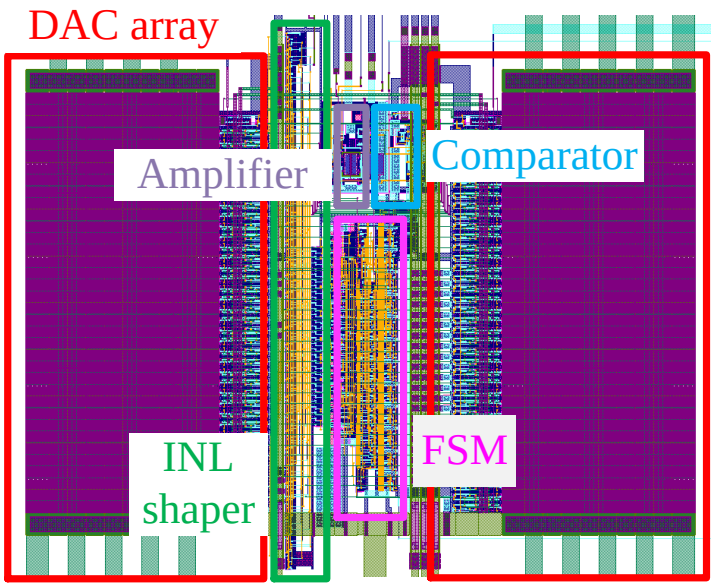



FIGURE 5.4. 2/4-fF MOM SAR ADC layout, dimensions: 370$\mu$m$\times$305$\mu$m = 0.11285 mm$^2$.

In the following sections the results obtained from the Prufpilo tests, such as DNL, INL and capacitors mismatch of each ADC are presented.

## 5.1. 10-bit SAR ADC results

Fig. 5.4 shows the layout of the SAR ADC using 2/4-fF MOM capacitors, and Fig. 5.5 shows the layout of the SAR ADC using 5-fF MIM capacitors. As explained in Chapter 3, the SAR ADC is composed by five different parts: a finite-state machine (FSM), which controls the ADC operation; two identical DAC arrays; a pre-amplifier, which reduces the noise and the offset; a latched comparator, responsible for the determination of the ADC output at every operation step; and an INL shaper, which is used to change the order in which the DAC capacitors are connected during a conversion. Moreover, not pointed out in the figures, there is also a double-phase clock generator in each ADC.

Fig. 5.6 and Fig. 5.7 show the measured DNL and INL of the 2-fF MOM SAR ADC and the 4-fF MOM SAR ADC, respectively, for the conditions indicated in Table 5.1.

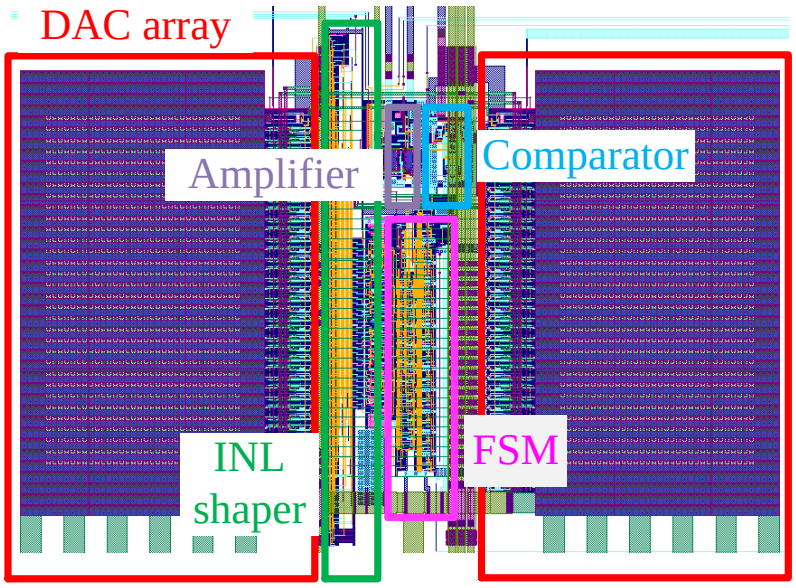



FIGURE 5.5. 5-fF MIM SAR ADC layout, dimensions: 445$\mu$m$\times$305$\mu$m = 0.135725 mm$^2$.

TABLE 5.1. SAR ADCs settings used for the tests.

| | 2-fF MOM | 4-fF MOM | 5-fF MIM | Comments |
|---|---|---|---|---|
| $V_{refp}$ [V] | 1.8 | 1.8 | 1.8 | ADC reference voltage |
| $V_{refm}$ [V] | 1.8 | 1.8 | 1.8 | ADC reference voltage |
| $V_{refcm}$ [V] | 0.9 | 0.9 | 0.9 | ADC reference voltage |
| $V_{ocm}$ [V] | 0.8 | 0.8 | 1.1 | Amp. output common-mode voltage |
| $V_{icm}$ [V] | 0.62 | 0.62 | 0.9 | ADC reference voltage |
| $f_{clk}$ [MHz] | 12.5 | 12.5 | 3.125 | Clock frequency |
| $R_{pol}$ [k$\Omega$] | 7 | 7 | 8 | Amp. bias-branch resistor |

After testing the 2-fF MOM SAR ADC and the 4-fF MOM SAR ADC for different INL shaper inputs, the results obtained were the same in all four cases. This is because, according to the information provided by the manufacturer about the process used, CMP steps are only applied to the via dielectric layers and not to the metal layers, hence the lateral-field MOM capacitors were not affected by radial effects due to copper dishing and

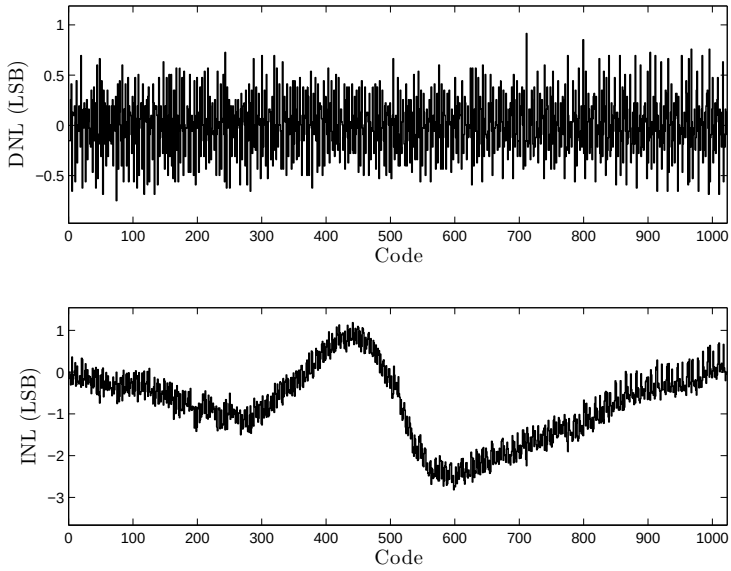



FIGURE 5.6. Measured DNL and INL of the 10-bit SAR ADC using 2-fF MOM capacitors. DNL = $0.9144/-0.7489$ and INL = $1.1877/-2.8183$.

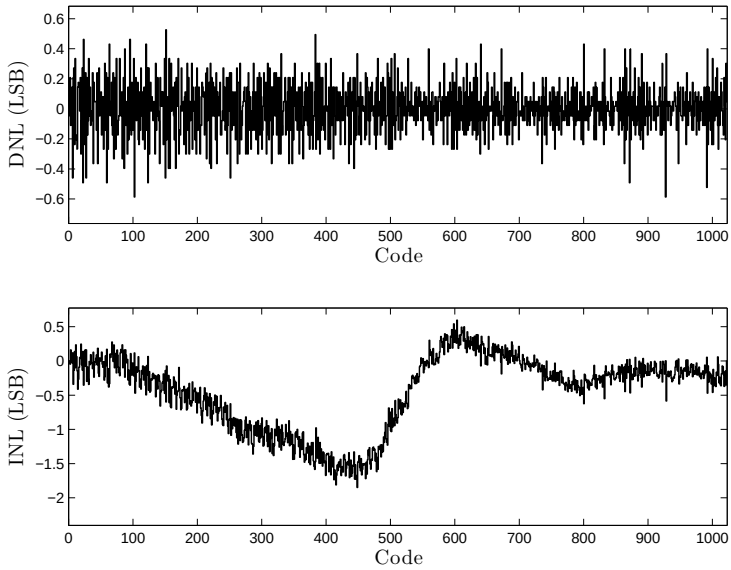
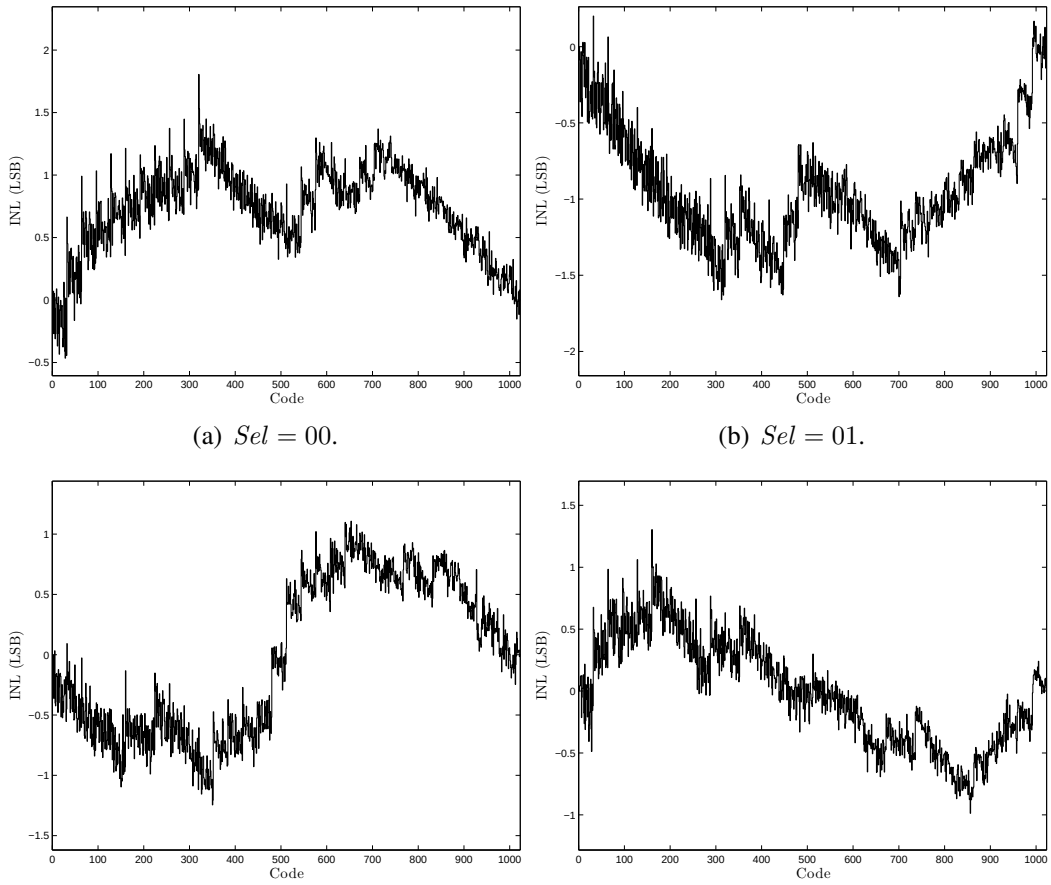



FIGURE 5.7. Measured DNL and INL of the 10-bit SAR ADC using 4-fF MOM capacitors. DNL = $0.5258/-0.58676$ and INL = $0.59569/-1.8478$.

the INL cannot be manipulated. This did not happen in the 5-fF MIM SAR ADC, where the capacitors were subject to radial effects due to gradients in the MIM capacitors dielectric layer. Fig. 5.8 shows the INL of the 5-fF MIM SAR ADC resulting from different INL shaper inputs for the conditions indicated in Table 5.1. The maximum and minimum DNL




(a) $Sel = 00$. (b) $Sel = 01$.

(c) $Sel = 10$. (d) $Sel = 11$.

FIGURE 5.8. Measured SAR ADC using MIM capacitors non-linearity resulting from different INL shaper inputs.

and INL obtained for each INL shaper input were: $Sel = 00$, DNL = $1.10890/-0.43343$ and INL = $1.80520/-0.46558$; $Sel = 01$, DNL = $0.73167/-0.49624$ and INL = $0.20154/-1.66080$; $Sel = 10$, DNL = $0.79564/-0.49596$ and INL = $1.10720/-1.24530$; and $Sel = 11$, DNL = $0.82629/-0.52768$ and INL = $1.30450/-0.98749$. The similarity between the results shown in Fig. 5.8 and the simulated results shown in Fig. 3.9 can be easily seen, which confirms the expected effects of radial effects during the fabrication process.

Finally, both input-referred noise and the unit capacitors mismatch were measured for each SAR ADC. The ADCs noise was measured by using the histogram technique (Ruscak

& Singer, 1995). Table 5.2 summarizes the results obtained for the conditions indicated in Table 5.1. It can be observed that the reported capacitors mismatch is consistent with the DNL and INL reported on Fig. 5.6 and Fig. 5.7, since the 4-fF MOM SAR ADC has a better DNL and INL than the 2-fF MOM SAR ADC because of the larger capacitances with lower mismatch. The 5-fF MIM SAR ADC cannot be fairly compared to the other two because its capacitors were affected by the copper dishing, altering the DNL and INL. The noise measurements using the histogram technique are sensitive to the ADC transfer characteristics, so the most accurate measurements correspond to those of the ADCs with larger capacitances, and hence lower mismatch and better DNL. The input-referred noise was also measured for different bias currents, and the results obtained show that the noise is limited by the pre-amplifier as expected.

TABLE 5.2. SAR ADCs input-referred noise and capacitors mismatch.

| ADC | Input-referred noise [LSBs] | Mismatch [%] |
|---|---|---|
| 2-fF MOM | 0.928 | 16.86 |
| 4-fF MOM | 0.531 | 11.38 |
| 5-fF MIM | 0.274 | 8.14 |

When testing all the SAR ADCs at $f_{clk} = 50$ MHz, none of them worked fine, and the transfer curves obtained presented lots of missing codes. Even though these ADCs were designed to operate at a clock frequency of $f_{clk} = 50$ MHz, the almost 1-centimeter long wire-bonds of the package introduce $\sim 10$ nH inductors in the supply and reference lines, limiting the chip maximum operation frequency. This was confirmed by simulation results including current limitations in the supply and reference lines.

Another problem observed during the tests was the occurrence of glitches in the transfer function of all the SAR ADCs for certain reference voltages and clock operation frequencies. Fig. 5.9 shows a transfer curve with glitches for illustration purposes. These glitches occurred for different input voltages, but they do not always occur, and there are some operation frequencies and reference voltages configurations that never show any

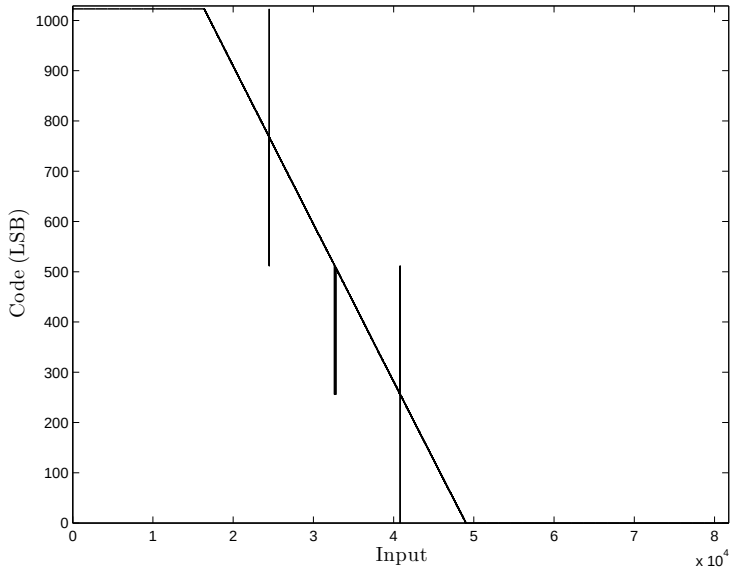



FIGURE 5.9. 5-fF MIM SAR ADC output to an input ramp.

glitches. The reason why these glitches occur is still under analysis, but there are some explanations that have been already discarded. For example, both noise and mismatch cannot be responsible for these glitches, since the former does not alter the transfer function in that way, and the later produces missing codes and alters the DNL and INL, but does not produce glitches. It could be considered that there are problems with the FSM design, but this alternative has been also discarded since there are operation points in which the ADCs work fine without glitches. Currently the most viable option under consideration is the occurrence of a race condition in the FSM. If a digital output depends on the state of the inputs, as the inputs vary, a delay will occur before the output changes, and for a brief period the output may change to an unwanted state. This condition may or may not affect the ADC operation by producing the glitches mentioned above, but testing this hypothesis is very difficult, and other possibilities should also be explored. Anyway, in order to definitely discard this alternative in a future version of the converter, dual-phase logic should be used.

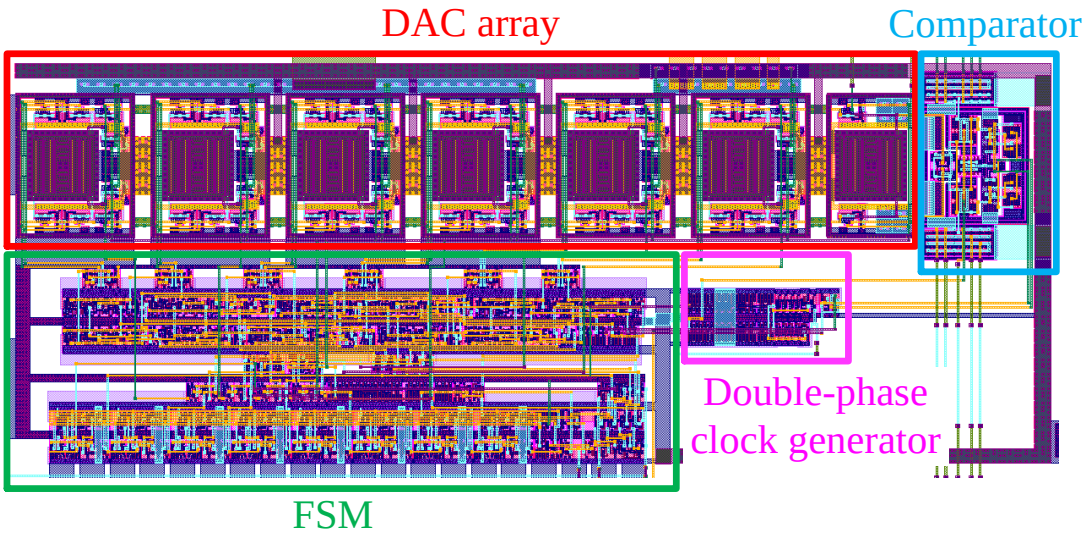



FIGURE 5.10. PRS ADC layout, dimensions: $210\mu\text{m}\times80\mu\text{m} = 0.0168$ mm$^2$.

## 5.2. PRS ADC results

Fig. 5.10 shows the layout of the PRS ADC using 100-fF MOM capacitors, and Fig. 5.11 shows a die micrograph of the actual PRS ADC implemented. As shown in Fig. 5.11, the PRS ADC is composed by four different parts: an FSM, which controls the ADC operation; a double-phase clock generator; a DAC array, which includes seven identical 100-fF capacitor structures along with their respective switches networks; and a latched comparator, responsible for the determination of the ADC output at every operation step. Only the capacitor structures can be recognized in the die micrograph of Fig. 5.11, the rest of the circuit was covered by dummy metal structures placed by the manufacturer. This converter features an area of only $0.0168$ mm$^2$, making it the smallest ADC among the different ADCs reported in a $0.18$ $\mu$m technology (Murmann, 2013).

As previously mentioned, the PRS ADC was implemented using a custom 100-fF MOM capacitor structure. This structure, shown in Fig. 5.12, is composed by two comb-shaped multi-layer metal structures in parallel, and was designed in order to obtain large

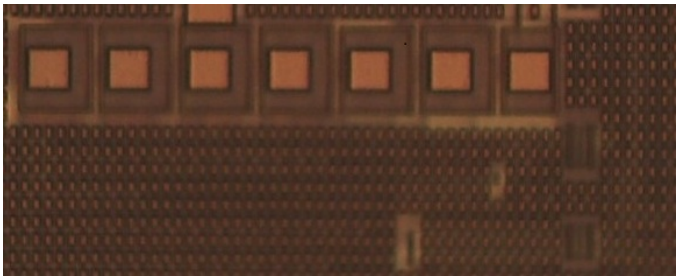


FIGURE 5.11. PRS ADC die micrograph.

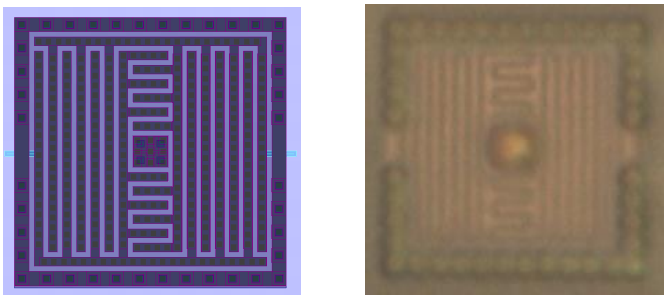


FIGURE 5.12. Layout top view and die micrograph of the custom 100-fF MOM capacitor used, dimensions: $14.265\mu$m$\times 14.18\mu$m$=202.3\mu$m$^2$.

and symmetrical parasitic capacitances to ground ($\sim$ 20 fF). This was achieved by surrounding the parallel metal structures with metal connected to ground. The structure capacitance and the parasitic capacitances to ground were extracted using Space 3D layout-to-circuit extractor software from Delft University (Van Genderen & Van der Meijs, 2000).

The measured DNL and INL of the PRS ADC are shown in Fig. 5.13, Fig. 5.14 and Fig. 5.15 for three different resolutions. These results were measured at an operation frequency of $f = 12.5$ MHz, and the reference voltages used for each measurement are specified in the figures captions. From these results, a mismatch of 26% for the custom 100-fF MOM capacitors was measured. This result, however, may also include somehow the parasitic capacitances to ground mismatch, since is too large for the capacitor metal structure used. Anyhow, in order to improve the PRS ADC performance (i.e., obtain

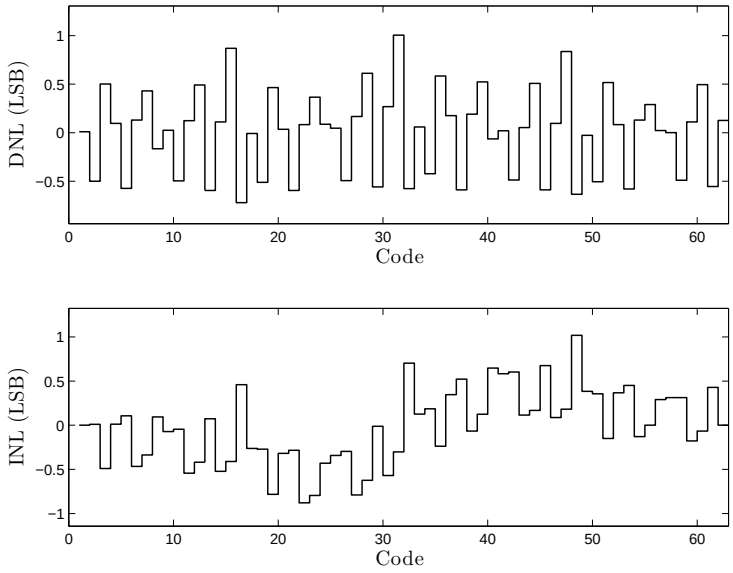



FIGURE 5.13. Measured DNL and INL of the PRS ADC (6 bits) for $V_{refp} = 1.2$ V, $V_{refm} = 0.6$ V and $V_{refcm} = 0.9$ V. DNL = $1.0045/-0.7207$ and INL = $1.0179/-0.8787$.

smaller absolute values for the DNL and INL), larger capacitors should be used, so that the mismatch is reduced. Also, instead of using larger capacitors, the use of MIM capacitors could be explored.

For the same conditions specified in Fig. 5.13, the ADC noise was measured by using the histogram technique (Ruscak & Singer, 1995), obtaining an input-referred noise of $0.175$ LSBs. Also, a power consumption of $156$ fJ/conversion-step was measured, without considering the double-phase clock generator consumption and the energy taken from the reference voltages. According to this result, the PRS ADC could work for 79 years with a single AAA battery. Of course, in order to make a fair comparison between the PRS ADC and other similar ADCs reported (Murmann, 2013), additional figures of merit should be computed first.

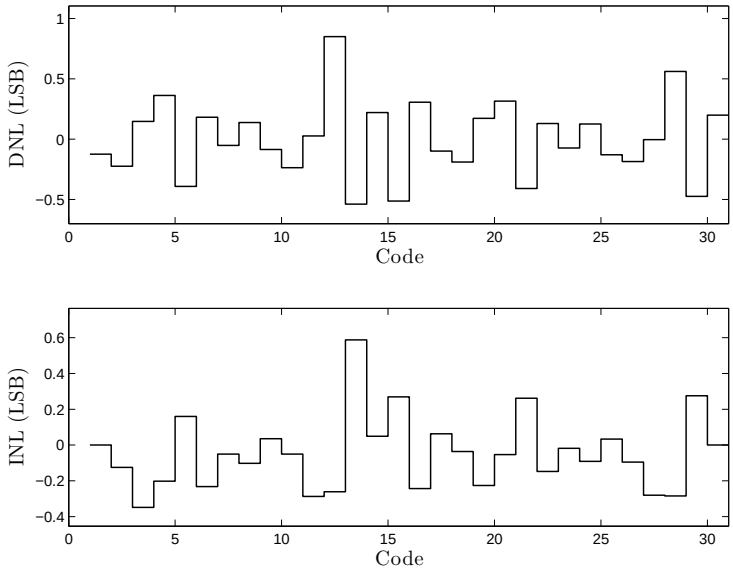



FIGURE 5.14. Measured DNL and INL of the PRS ADC (5 bits) for $V_{refp} = 0.95$ V, $V_{refm} = 0.85$ V and $V_{refcm} = 0.9$ V. DNL = $0.8494/-0.5387$ and INL = $0.5880/-0.3489$.

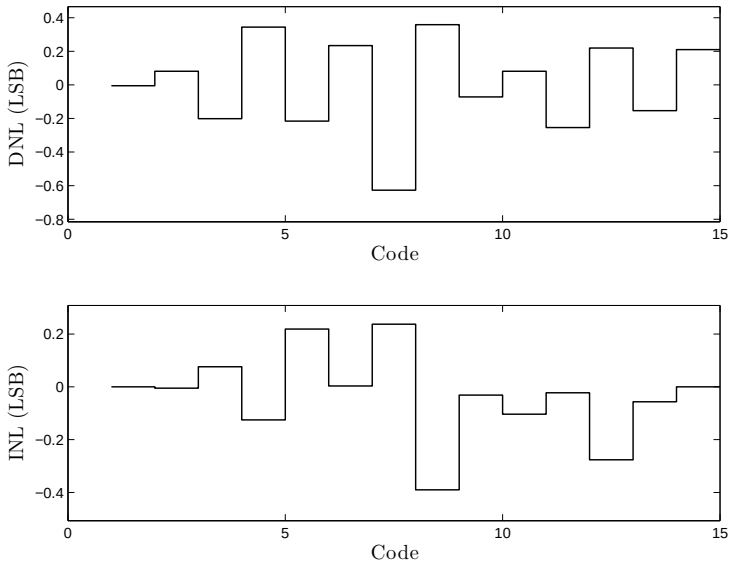



FIGURE 5.15. Measured DNL and INL of the PRS ADC (4 bits) for $V_{refp} = 0.92$ V, $V_{refm} = 0.88$ V and $V_{refcm} = 0.9$ V. DNL = $0.3584/-0.6269$ and INL = $0.2371/-0.3898$.

# 6. CONCLUSION

This thesis presents the use of CMOS techniques in integrated circuits for particle physics experiments. In general terms, this work includes a new approach for noise analysis in charge-sense amplifiers based on an extension of the $g_m/I_D$ methodology, the design, implementation and test results of a 10-bit SAR ADC with configurable INL for the BeamCal IC, and the presentation of a new passive-reference sharing ADC architecture, along with its implementation and test results.

The noise analysis methodology introduced in this work provides a new insight on the impact of flicker noise in electronic systems for radiation detection, evidences that flicker noise is related with the existence of a finite current for which noise is minimum, and also outlines the relation between flicker noise and the filter peaking time.

The fully-differential SAR ADC with configurable INL for the BeamCal IC has been also presented, along with its test results using different capacitor structures. This converter features a manipulable INL, which allows to compensate the non-linearity of the circuits connected to the ADC taking advantage of the otherwise detrimental radial effects during the fabrication process.

Finally, a new fully-differential PRS ADC architecture was introduced, along with its noise and non-idealities analysis, simulations and test results. This converter features a capacitance spread of one, a very small area, a low-power consumption and a reconfigurable resolution.

In this work, a sub-optimal microelectronic design flow was achieved, regardless of the problems introduced by the use of the manufacturer libraries for the schematic and layout editor used. A typical design flow comprises the schematic design, schematic simulations, layout edition, parasitics extraction and post-layout simulations including the extracted parasitics components. Due to the problems introduced by the use of the manufacturer libraries, the parasitics extraction and post-layout simulation could not be completed. Also, because of some inconsistencies in the schematic simulator used, the

schematic simulations including the pads could not be carried out either. Regardless of these various problems, the main points of this work were successfully proven, since it was shown that the INL of a SAR ADC can be manipulated taking advantage of the position of the DAC array capacitors and the radial effects, and also the viability of the PRS ADC was proved by fabricating the ADC as a proof of concept, and showing that this architecture is promising in terms of die area, simplicity and power consumption.

## 6.1. Future work

During the development of this work, a different technology to be used for the FONDECYT project described in Chapter 1 has been chosen, so the 10-bit SAR ADC will have to be re-designed, implemented and characterized. Moreover, the software to be used for the IC design has also changed, so the full design flow should be implemented including parasitics extraction ans post-layout simulations.

Considering the recent changes that have been made in the FONDECYT project, first of all, the origin of the glitches mentioned in Chapter 5 should be determined in order to correct this problem in future versions of the 10-bit SAR ADC. Moreover, the characterization of the SAR ADCs implemented should be finished, including the tests of the power-saving operation mode. Also, the noise analysis technique introduced in this work should be tested with an actual design of the CSA to be included in the BeamCal IC, in order to validate the presented results and strengthen the proposed approach.

Finally, the PRS ADC limits should be further explored, and its performance should be evaluated using a lower power supply and higher clock frequencies. In order to publish the results obtained with this work, the characterization of the PRS ADC should be also finished by computing some relevant figures of merit.

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# APPENDIX

# APPENDIX A. ADDITIONAL RESOURCES

The Prufpilo IC has 84 pads and was bonded to an 84-lead PLCC package. Table A.1 shows the Prufpilo pinout.

Table A.1: Prufpilo IC pinout.

| Pin Nº | Pin name | Description |
|---|---|---|
| 1 | NB2_PRS | PRS ADC number of bits selector |
| 2 | NB1_PRS | PRS ADC number of bits selector |
| 3 | VDD3.3_PRS | PRS ADC 3.3 V digital power supply |
| 4 | VDD1.8_PRS | PRS ADC 1.8 V digital power supply |
| 5 | E_PRS | PRS ADC enable signal |
| 6 | clk_PRS | PRS ADC clock |
| 7 | DGND | Digital ground |
| 8 | B_PRS | PRS ADC serial output |
| 9 | C25 | PRS ADC comparator calibration |
| 10 | C24 | PRS ADC comparator calibration |
| 11 | C23 | PRS ADC comparator calibration |
| 12 | C22 | PRS ADC comparator calibration |
| 13 | C21 | PRS ADC comparator calibration |
| 14 | C15 | PRS ADC comparator calibration |
| 15 | C14 | PRS ADC comparator calibration |
| 16 | C13 | PRS ADC comparator calibration |
| 17 | C12 | PRS ADC comparator calibration |
| 18 | C11 | PRS ADC comparator calibration |
| 19 | NC | No connection |
| 20 | NC | No connection |

| | | |
|---|---|---|
| 21 | NC | No connection |
| 22 | NC | No connection |
| 23 | NC | No connection |
| 24 | NC | No connection |
| 25 | NC | No connection |
| 26 | NC | No connection |
| 27 | NC | No connection |
| 28 | NC | No connection |
| 29 | NC | No connection |
| 30 | NC | No connection |
| 31 | NC | No connection |
| 32 | NC | No connection |
| 33 | AVDD1.8_MOM2 | 4-fF MOM SAR ADC 1.8 V analog power supply |
| 34 | AGND | Analog ground |
| 35 | VDD1.8_MOM2 | 4-fF MOM SAR ADC 1.8 V digital power supply |
| 36 | vm_MOM2 | 4-fF MOM SAR ADC input signal |
| 37 | vp_MOM2 | 4-fF MOM SAR ADC input signal |
| 38 | VDD3.3_MOM2 | 4-fF MOM SAR ADC 3.3 V digital power supply |
| 39 | DGND | Digital ground |
| 40 | clk_MOM2 | 4-fF MOM SAR ADC clock |
| 41 | pN_MOM2 | 4-fF MOM SAR ADC amplifier polarization input |
| 42 | pP_MOM2 | 4-fF MOM SAR ADC amplifier polarization input |
| 43 | B_MOM2 | 4-fF MOM SAR ADC serial output |
| 44 | DGND | Digital ground |
| 45 | DGND | Digital ground |
| 46 | clk_MIM | 5-fF MIM SAR ADC clock |
| 47 | pN_MIM | 5-fF MIM SAR ADC amplifier polarization input |

| | | |
|---|---|---|
| 48 | pP_MIM | 5-fF MIM SAR ADC amplifier polarization input |
| 49 | vm_MIM | 5-fF MIM SAR ADC input signal |
| 50 | vp_MIM | 5-fF MIM SAR ADC input signal |
| 51 | B_MIM | 5-fF MIM SAR ADC serial output |
| 52 | AGND | Analog ground |
| 53 | AVDD1.8_MIM | 5-fF MIM SAR ADC 1.8 V analog power supply |
| 54 | DGND | Digital ground |
| 55 | VDD1.8_MIM | 5-fF MIM SAR ADC 1.8 V digital power supply |
| 56 | VDD3.3_MIM | 5-fF MIM SAR ADC 3.3 V digital power supply |
| 57 | DGND | Digital ground |
| 58 | clk_MOM | 2-fF MOM SAR ADC clock |
| 59 | vm_MOM | 2-fF MOM SAR ADC input signal |
| 60 | vp_MOM | 2-fF MOM SAR ADC input signal |
| 61 | B_MOM | 2-fF MOM SAR ADC serial output |
| 62 | AGND | Analog ground |
| 63 | AVDD1.8_MOM | 2-fF MOM SAR ADC 1.8 V analog power supply |
| 64 | DGND | Digital ground |
| 65 | VDD1.8_MOM | 2-fF MOM SAR ADC 1.8 V digital power supply |
| 66 | VDD3.3_MOM | 2-fF MOM SAR ADC 3.3 V digital power supply |
| 67 | vrefn_SAR | SAR ADCs reference voltage |
| 68 | vrefcm_SAR | SAR ADCs reference voltage |
| 69 | vicm_SAR | SAR ADCs reference voltage |
| 70 | vocm_SAR | SAR ADCs reference voltage |
| 71 | vrefp_SAR | SAR ADCs reference voltage |
| 72 | INL1_sel | SAR ADCs INL shaper selector |
| 73 | INL2_sel | SAR ADCs INL shaper selector |
| 74 | PCy | SAR ADCs power cycling selector |

| | | |
|---|---|---|
| 75 | E_SAR | SAR ADCs enable signal |
| 76 | DGND | Digital ground |
| 77 | pN_MOM | 2-fF MOM SAR ADC amplifier polarization input |
| 78 | pP_MOM | 2-fF MOM SAR ADC amplifier polarization input |
| 79 | DGND | Digital ground |
| 80 | vrefp_PRS | PRS ADC reference voltage |
| 81 | vrefcm_PRS | PRS ADC reference voltage |
| 82 | vrefn_PRS | PRS ADC reference voltage |
| 83 | vp_PRS | PRS ADC input signal |
| 84 | vm_PRS | PRS ADC input signal |

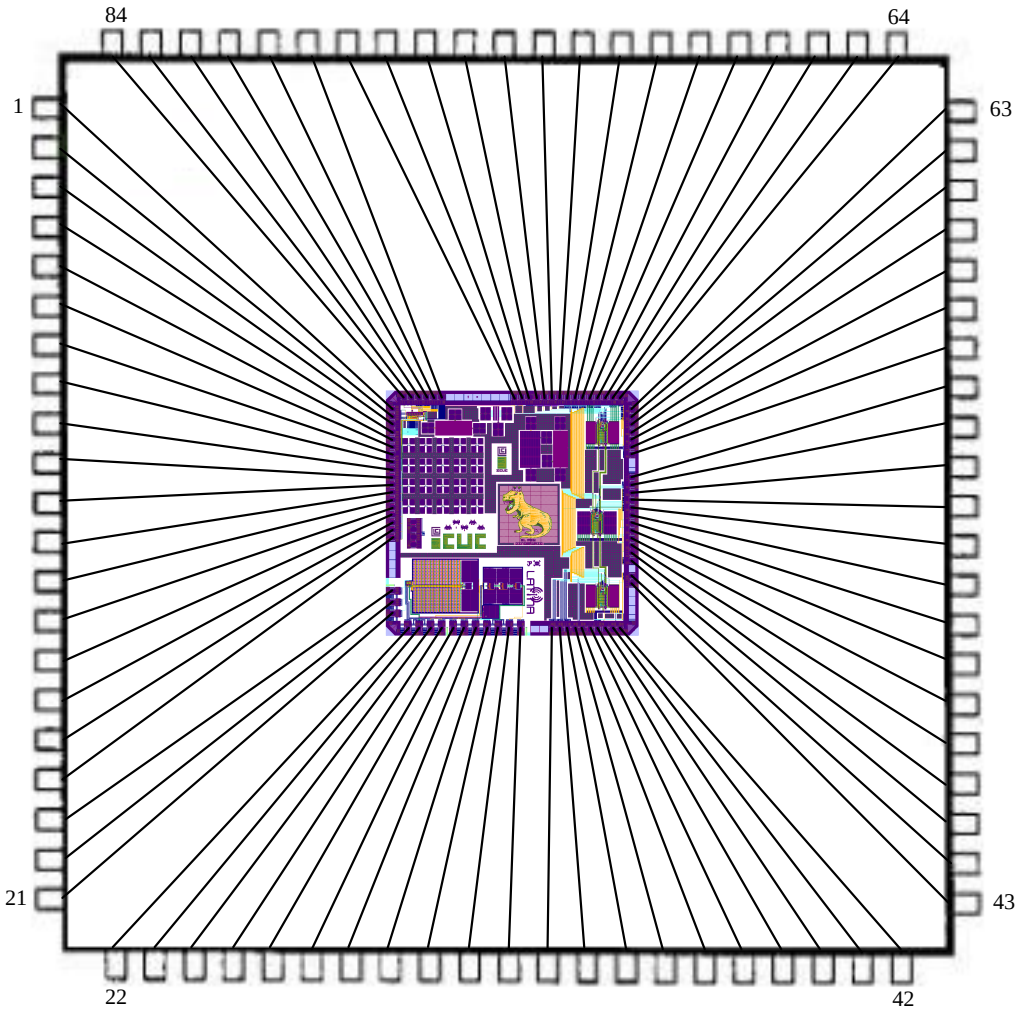


FIGURE A.1. Prufpilo bonding diagram.