PONTIFICIA UNIVERSIDAD CATOLICA DE CHILE
SCHOOL OF ENGINEERING

PASSIVE REFERENCE-SHARING SAR ADC FOR ULTRA LOW POWER APPLICATIONS

MATÍAS JARA TORO

Thesis submitted to the Office of Research and Graduate Studies
in partial fulfillment of the requirements for the degree of
Master of Science in Engineering

Advisor:
ANGEL ABUSLEME HOFFMAN

Santiago de Chile, January 2016

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To my parents, my family, and Ximena, for their support and unconditional love.

ACKNOWLEDGEMENTS

I would like to thank my advisor, Professor Angel Abusleme, for being an amazing mentor, for saving Chile by bringing the microelectronics field, and for giving me the opportunity to work with him in the design of integrated circuits. Thanks for his continued technical and research guidance throughout these years. Without his advice this work would not be the half of what it is. I hope to follow his steps, and struggle for the microelectronic industry growth in this country.

I wish to thank all the members of IC-UC for being an incredible research group and helping me with rewarding discussions. Special mentions to Enrique Alvarez for letting me to continue his work and giving me valuable advice in the first period of my thesis, Cristóbal Alessandri for his constant help with the EDA softwares tools, and Juan Andrés Bozzo for being the best tech support ever and taking good care of MEGATRON. In addition, I want to thank Joaquin Venegas of LATINA, for helping me with the digital design flow and the Synopsys tools.

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ABSTRACT

The passive reference-sharing (PRS) is a novel topology for successive approximation register (SAR) analog-to-digital converters (ADC) that employs equally sized capacitors in the digital-to-analog converter (DAC) array. This characteristic allows a smaller die area and high energy efficient operation for medium resolution converters. A complete review of a PRS SAR ADC is presented in this work, analyzing its design-space and performance bounds. Based on the analysis, an optimized design for an 8-bit ADC is proposed and implemented using a 0.13 μm technology process, with a die area of 0.024 mm^2. Post-layout simulations results report a figure of merit (FOM) of 35.4 fJ/conv-step, an effective number of bits (ENOB) of 7.32 bits, and a power consumption of 11.78 μW at a sampling rate of 2.08 MS/s. This features make the proposed design suitable for ultra low power applications, such as wireless sensor nodes and biomedical devices. Finally, a chip was submitted for fabrication to measure the actual performance of the proposed converter.

Keywords: Analog-to-digital converter (ADC), low power integrated circuits, **successive approximation register (SAR), passive reference sharing (PRS)**.

RESUMEN

La compartición pasiva de referencia (PRS) es una reciente topología para conversores análogo-digital (ADC) de registro de aproximaciones sucesivas (SAR) que emplea capacitores de igual tamaño para el arreglo del conversor digital-análogo (DAC). Esta característica permite utilizar áreas menores de silicio y operar con una gran eficiencia energética en conversores de resolución media. En este trabajo se presenta un completo estudio del PRS SAR ADC, analizando su espacio de diseño y los límites del desempeño. Basado en este análisis, se propone e implementa un diseño óptimo para un ADC de 8 bits utilizando un proceso tecnológico de 0.13 μm, con una superficie total de 0.024 mm^2. Resultados de simulaciones reportan una cifra de mérito (FOM) de 35.4 fJ/conv-step, un número efectivo de bits (ENOB) de 7.32 bits y un consumo total de 11.78 μW empleando una frecuencia de muestro de 2.08 MS/s. Estas cifras hacen que el conversor de datos propuesto sea apto para su uso en aplicaciones de bajo consumo de potencia, tales como redes de sensores inalámbricos y dispositivos biomédicos. Por último, un chip fue enviado a fabricar para medir el desempeño real del conversor propuesto.

Palabras Claves: conversor analógo-digital (ADC), circuito integrados de baja potencia, **registro de aproximaciones sucesivas (SAR), compartición pasiva de refencia (PRS)**.

1. INTRODUCTION

1.1. Integrated Circuits for Ultra Low Power Applications

The low cost of semiconductor manufacturing and the design of high-performance integrated circuits have allowed to develop many novel electronic devices, which have revolutionized the computer, biomedical and communication industries. Moreover, this technology growth has given birth to wireless devices that have become essential tools in our days, such as smartphones and tablet computers. Since these devices require a power source, in most cases they use rechargeable batteries. However, there are some wireless devices that can not admit bulky batteries and others that require long term energy autonomy. Therefore, the development of low power integrated circuits with inexhaustible power source has became an attractive research topic. Some examples of low power wireless devices are wireless sensor networks (WSN) and body sensor networks (BSN) (Akyildiz, Su, Sankarasubramaniam, & Cayirci, 2002). In addition, biomedical systems on a chip (SoC) have been implemented for heart disorders monitoring (Jeon et al., 2014) and for implantable peacemakers (Wong et al., 2004).

The main objetive of the applications mentioned above is to sense or detect nature behaviours, such as environmental variables for weather forecast or biological signals for biomedical devices, thus ultra low power data converter are required to relax the circuit limitation on the power budget constraint (Calhoun et al., 2005). In addition, for biomedical integrated circuits the die size must be minimized too (Wu, 2010). On the other hand, frequency and resolution of the sensing variables are not critical in these applications, many low-frequency and medium resolution ADC have been studied in order to reach ultra low-power consumption (Kamalinejad, Mirabbasi, & Leung, 2011; Zhang, Bhide, & Alvandpour, 2012; Jeong et al., 2015).

In this work an energy-efficient ADC is revised in order to optimize the performance of the converter, minimizing the power consumption and maximizing the resolution and speed.

1.2. Analog-to-Digital Converters Overview

An analog-to-digital converter (ADC) is a circuit that convert a voltage signal to a binary sequence. In modern electronics, all the storage of information and its processing is performed in the digital domain, thus data converters are critical elements to connect the physical world to the digital domain (Pelgrom, 2010). In the last 40 years, data converters have been deeply studied and the demand for high-performance devices keeps growing.

1.2.1. Analog-to-digital Nomenclature

For an ideal ADC the ramp response is a staircase function as the one shown in Figure 1.1. The ideal step width is defined as the least significant bit (LSB) size, expressed as:[1] $\mathrm{LSB} = \mathrm{FSR}/2^B$, where the FSR term is the full scale range voltage and B is the bit resolution. Also, each k-th output code of an ADC has a transition level (T_k) defined as the transition input voltage between digital codes k and $k+1$. From this, the k-th code width (W_k) is defined as the difference between transitions T_k and T_{k+1}.

1.2.1.1. Non-linearities

In a real implementation the width of each step in the static transfer curve is not uniform, which is caused by intrinsic non-linearities of the circuit. Figure 1.2 shows an example of a 3-bit ADC including non-linearities.

To quantify the non-linearities, two performance metrics are defined: the integral non-linearity error (INL) and the differential non-linearity error (DNL). These metrics do not consider offset or a gain error, (Figure 1.3), because linearity is not affected by them.

Differential Non-linearity

The DNL is the difference between a specific width and its ideal value, normalized to the LSB value. From this, the DNL of the k-th code is written as (Maloberti, 2007)

$$\mathrm{DNL}(k) = \frac{W_k - W_{ideal}}{\mathrm{LSB}}. \tag{1.1}$$

[1] This equation is only valid for a bipolar quantizer (Kester & Analog Devices, 2005)

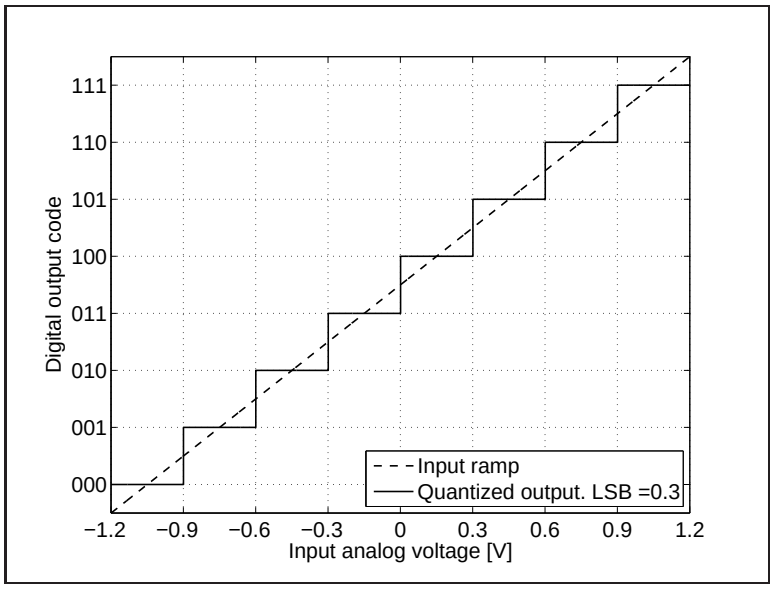


FIGURE 1.1. Transfer function of an ideal 3-bit ADC. Using a bipolar mid-rise convention and FSR=2.4 V.

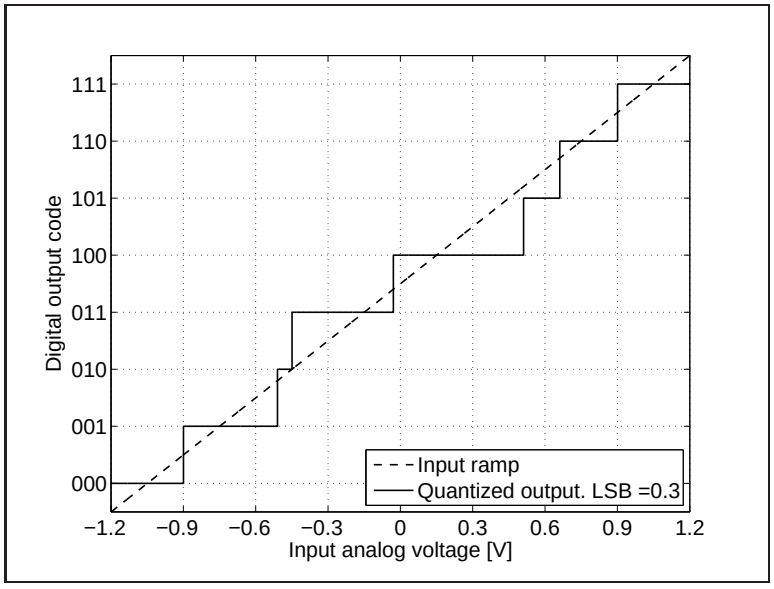


FIGURE 1.2. Transfer function of a 3-bit ADC with non-linearities. Using a bipolar quantizer and FSR=2.4 V.

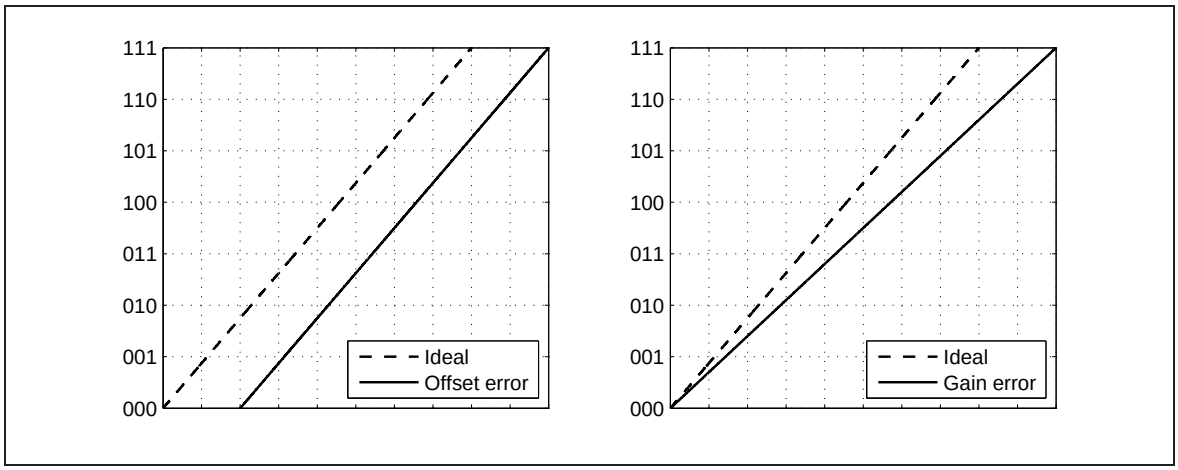


FIGURE 1.3. Offset and gain error on static curve. Using a 3-bit bipolar quantizer.

Using (1.1), the calculated DNL for each code of the 3-bit example of Figure 1.2 is shown in Figure 1.4. If the DNL is -1, it means that a code is missing. Also, the accumulated sum of the DNL must be zero, and as the offset and gain error are assumed to be corrected, the first and last codes have an undefined DNL value.

Integral Non-linearity

The INL is the difference between a specific transition and the ideal value, normalized to the LSB value. In other words, the INL is the difference between each point of the transfer function and the ideal, straight line function. The INL of the k-th code is written as (Maloberti, 2007)

$$\mathrm{INL}(k) = \frac{T_k - T_{k,ideal}}{\mathrm{LSB}}. \tag{1.2}$$

Using (1.2), the INL is computed for the 3-bit example of Figure 1.2. The results for each code are shown in Figure 1.5. If the difference between two continuous INL values is below -1, it means that a code is missing. Sometimes the DNL does not reveal these errors, because the DNL is susceptible to thermal noise, but the INL, being an accumulative metric is insensitive to thermal noise. Additionally, the first value is undefined, and as the offset and gain error are assumed to be corrected, the second and last code have zero value.

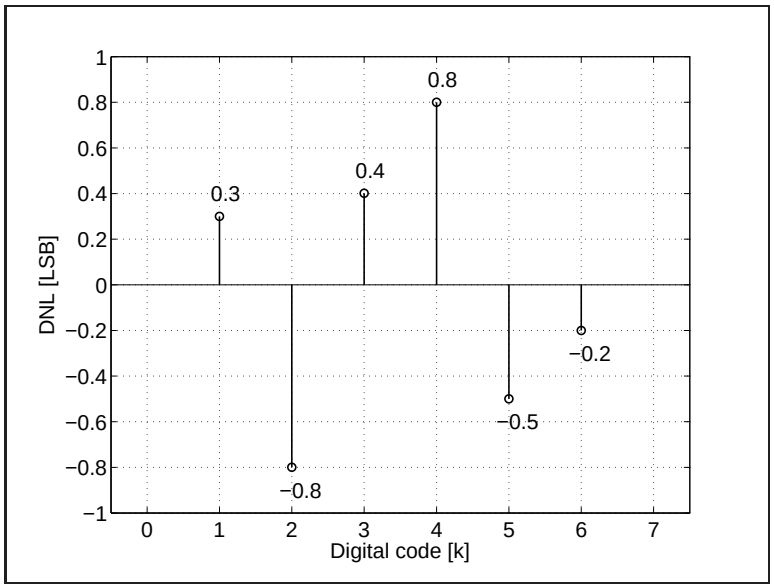


FIGURE 1.4. Differential non-linearity for a 3-bit ADC example. LSB = 0.3 V.

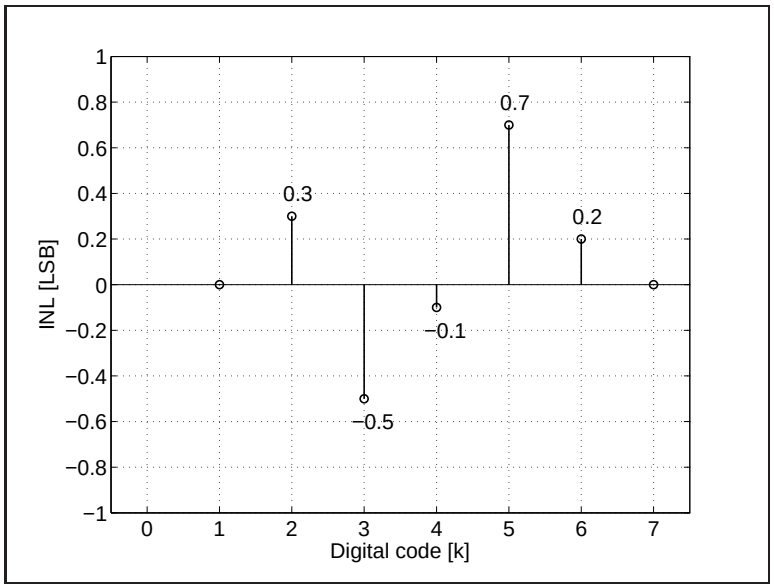


FIGURE 1.5. Integral non-linearity for a 3-bit ADC example. LSB = 0.3 V.

1.2.2. Trends of Analog-to-Digital Converters

Depending on the application, many ADC topologies have been studied and discussed in the literature. The main characteristics of an ADC are defined in term of its resolution (B), sampling frequency (f_s), power consumption (P) and signal-to-noise and distortion ratio (SNDR). The latter reveals the effective number of bits (ENOB) and provides an assessment of the linearity in a dynamic approach.

The first difference between converter topologies is the sampling frequency: Nyquist-rate ADCs and oversampling ADCs. In the first group, flash ADCs, successive approximation register (SAR) ADCs and pipeline ADCs are the most typical. In the second group sigma-delta ($\Sigma\Delta$) ADCs are the most popular. Each of these ADC's have different characteristics and limitations. Figure 1.6 and 1.7 show a survey of different architectures. These plots reveals that $\Sigma\Delta$ ADCs reach higher resolutions at the expense of high power consumption and low-medium operation frequency; flash ADCs can handle higher operation frequency than other architectures, at the expense of high power consumption and limited resolution. Pipeline ADCs have medium to high resolution and medium to high operation frequency, at the expense of medium power consumption and high implementation complexity. Finally, SAR ADCs are the most efficient in term of power consumption, at the expense of medium resolution and relatively low operation frequency.

In the particular case of low power applications, such as sensor nodes, the sensed signals have slow variations and usually do not need high resolutions. Therefore, SAR ADCs are the most suitable converter architecture in these cases (Calhoun et al., 2005).

1.2.2.1. Figure of Merits

To compare different ADCs, performance metrics have been proposed. These figures of merit (FOM) are based on ADC trends, observed through survey data and operation. The most typical are the Walden (Walden, 1999) and Schreier (Schreier & Temes, 2004) FOMs. The Walden FOM, measured in fJ per conversion step, suggest two trends. First, in order to increase the sampling rate, the power consumption must be increased in the same amount. Second, in order to increase the resolution by one, the power consumption must

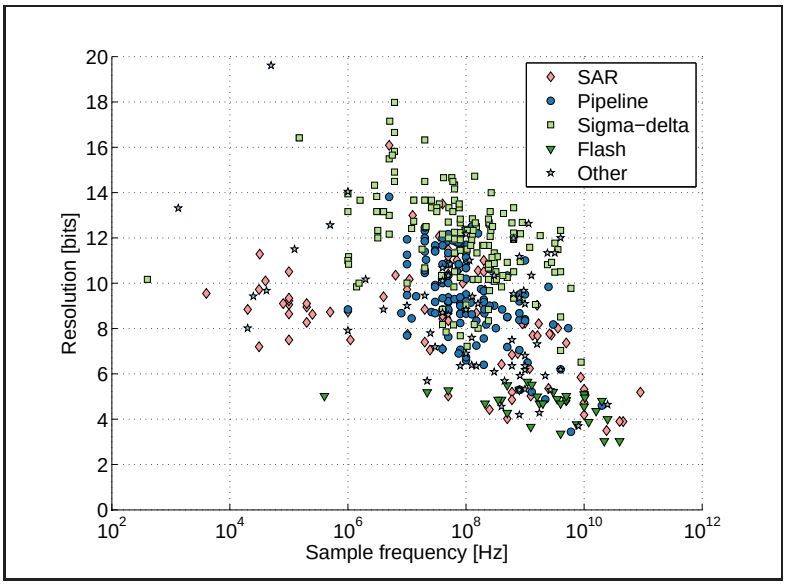


FIGURE 1.6. Resolution versus sampling frequency ADC survey from ISSCC and VLSI conferences between 1997 and 2015 (Murmann, 2015).

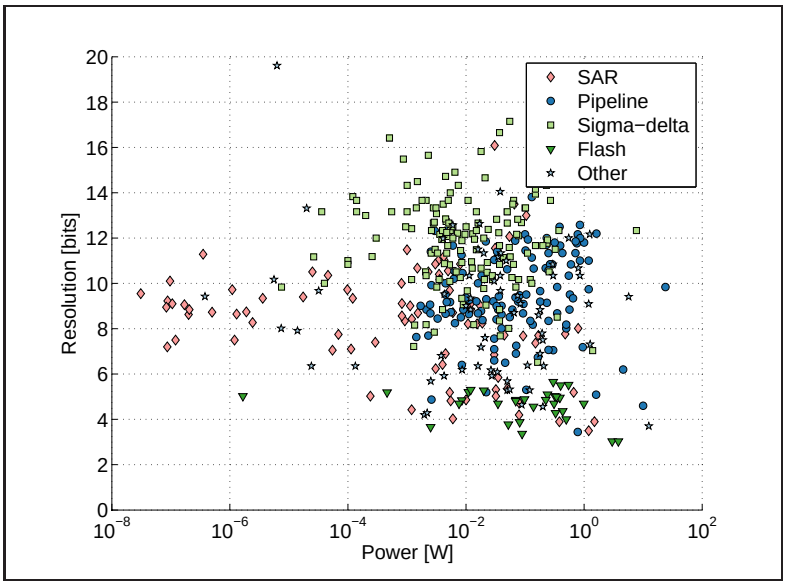


FIGURE 1.7. Resolution versus power consumption ADC survey from ISSCC and VLSI conferences between 1997 and 2015 (Murmann, 2015).

be increased by a factor of 2. From this, Walden FOM is defined as

$$\mathrm{FOM_W} = \frac{P}{2^{\mathrm{ENOB}} f_s}. \tag{1.3}$$

The Walden FOM works well when the power is not limited by noise, which is the case when the circuit is almost entirely digital. To include the thermal noise in the performance metric, the Schreier FOM suggests the same trend, but considering the SNDR squared. This modification arises because in many analog applications, such as a common source stage, in order to reduce the thermal noise by 6dB the power must increase in a factor of 4. In logarithmic form, the Schrerier FOM is defined as

$$\mathrm{FOM_S} = \mathrm{SNDR(dB)} + 10\log_{10}\left(\frac{f_s}{P}\right). \tag{1.4}$$

There is no FOM that ensures a fair comparison between all the ADC topologies, however the Walden FOM is the most used, because power versus speed at the same SNDR is a suitable performance metric in energy terms. Using these metrics, (Murmann, 2015) performed an energy comparison of many ADCs. Figure 1.8 shows the result of his survey.

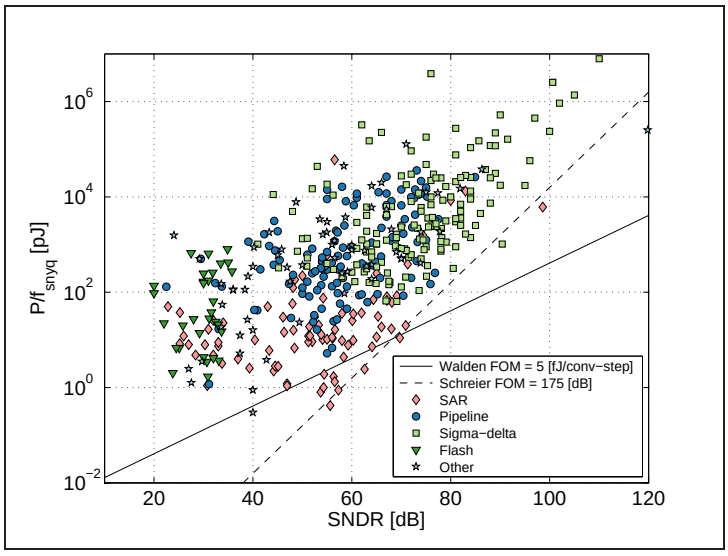


FIGURE 1.8. Comparison in terms of energy ADC survey from ISSCC and VLSI conferences between 1997 and 2015, including Walden and Schreier FOMs .

1.3. The Successive Approximation Register ADC Architecture

In order to classify a random value, one viable alternative is to use dichotomic search (P. E. Black, 2004). The successive approximation register (SAR) algorithm quantizes the analog input value by carrying out a search based on choosing between two alternatives on sequentially.

The conversion is done as follows. In the first cycle, the most significant bit (MSB) is the result of comparing the input voltage and $V_{ref}/2$ threshold. In the next cycle, depending on the MSB value, a new threshold voltage is set either at $V_{ref}/4$ or $3V_{ref}/4$ value if the computed MSB is 0 or 1, respectively. Then, the input signal is again compared with the new threshold voltage to obtain the next bit. This two steps are repeated until the difference between the input voltage and the threshold value converges to zero and all the bits of the quantized output are obtained. Thus, for a B bit result, a minimum of B cycles are needed. This limits the SAR ADC conversion rate. Figure 1.10 shows some examples for a 3-bit SAR ADC where 4 cycles per conversion are needed. A typical implementation of a SAR ADC uses three basic blocks: a DAC to provide the current guessed value, a comparator to compare the input with the guessed voltages, and a digital logic block to control the conversion. This is shown in Figure 1.9.

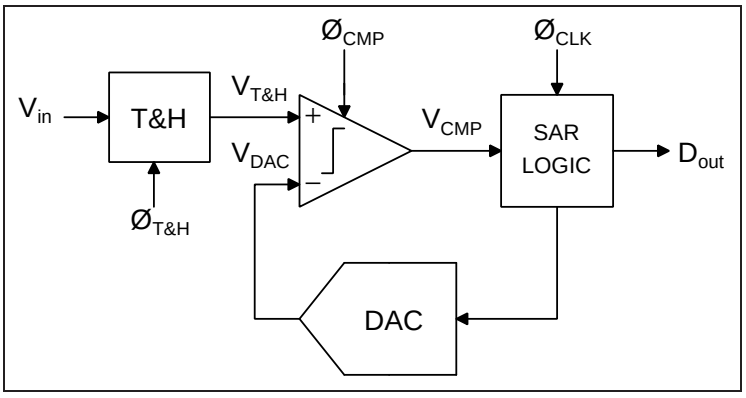
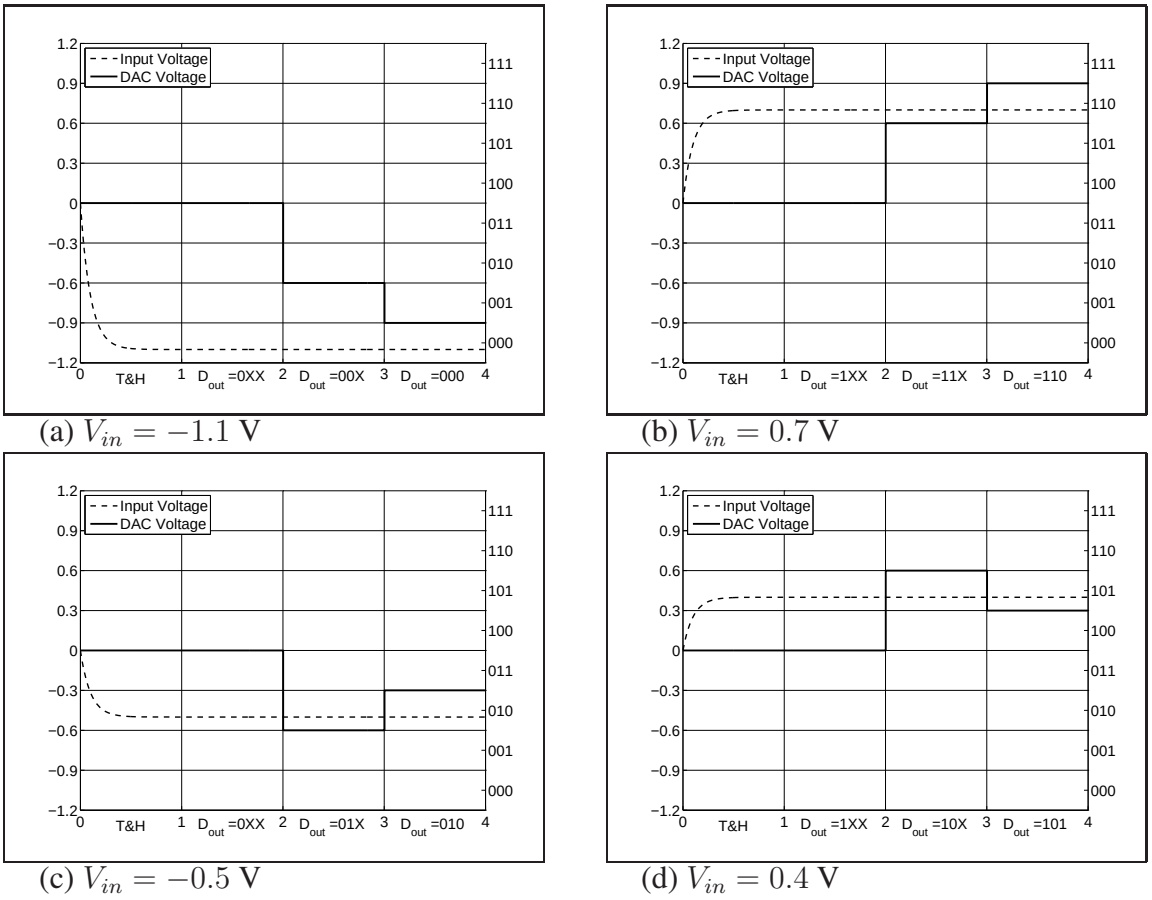


FIGURE 1.9. Generic SAR ADC block diagram.



(a) $V_{in} = -1.1$ V (b) $V_{in} = 0.7$ V

(c) $V_{in} = -0.5$ V (d) $V_{in} = 0.4$ V

FIGURE 1.10. 3-bit SAR ADC flow diagram example. With FSR = 2.4 V and bipolar quantizer.

In (McCreary & Gray, 1975) a SAR ADC using an active charge redistribution implementation was introduced. This implementation is detailed in the literature (Maloberti, 2007; Pelgrom, 2010) as the basic implementation of a SAR ADC. As the comparator and the digital logic can be designed to have a negligible static power dissipation, having a DAC implementation based on charge redistribution reduces significantly the power consumption, which is dominated by the capacitor size. This is why SAR ADC have been the most efficiently ADC in terms of energy.

1.3.1. The Passive Charge-Sharing Algorithm

In (Craninckx & Van der Plas, 2007) an energy-efficient SAR ADC was proposed using a passive charge-sharing process instead of an active charge redistribution, as shown

in Figure 1.11. The operation of the circuit is as follows: after the sampling capacitor C_s is reset to zero through switches S_r, all the DAC capacitors are charged with the voltage reference and the input voltage is stored in the sampling capacitors through switches S_c and S_s, respectively. If the input voltage is positive, then the comparator outputs a high value ($D_{\text{out}} = 1$) and in the next step, the leftmost capacitor of the array is connected inversely through switches $S_{m,B-1}$. This results in a passive subtraction. On the other hand, if the input voltage is negative, then the comparator outputs a low value ($D_{\text{out}} = 0$) and in the next step, the leftmost capacitor of the array is connected directly through switches $S_{p,B-1}$. This results in a passive addition. At the end of the step the comparator makes a new decision based upon the result of the passive charge-sharing process. Then, this process is repeated, connecting the remaining capacitors, until all the bits are obtained. The DAC capacitor array must be binary sized to ensure a binary search algorithm.

As the DAC capacitors are only charged at the beginning of each conversion, the energy consumed by the capacitor array is reduced significantly.

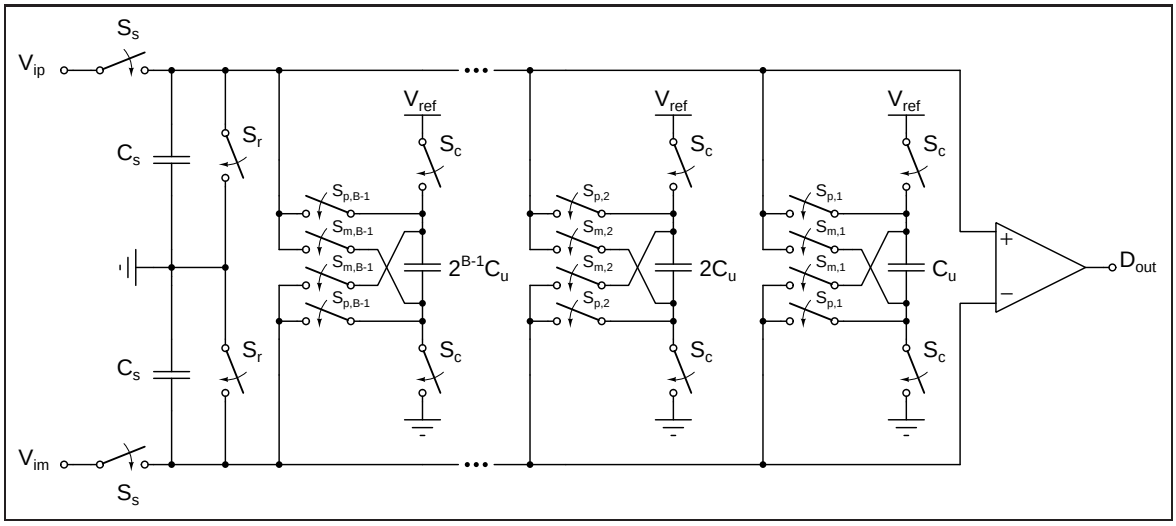


FIGURE 1.11. Simplified passive charge-sharing SAR ADC architecture.

1.4. The Passive Reference-Sharing Algorithm

To reduce the DAC capacitor die area and capacitance spread[2], a passive reference sharing (PRS) algorithm was proposed in (Alvarez-Fontecilla & Abusleme, 2015). It uses the passive charge-sharing principle, but each capacitor in the array has the same size. The PRS algorithm consists of two concurrent processes: the reference-sharing (RS) and the successive approximation (SA).

At the beginning of the conversion, when a differential analog input is sampled, two capacitors are charged with a differential reference voltage, while all the other capacitors are charged with cero differential potencial. Then, the comparator makes a decision from the differential input voltage. Depending on the comparator output value, in the next step, the first capacitor is connected to the adjacent capacitor directly or inverted, thus an addition or a subtraction is done between a reference voltage and the voltage in the comparator input. Then, the comparator makes a new decision from the resulting voltage at the comparator input. This operation continues for each bit, converging to zero as in a successive approximation process, but using only the energy of two capacitors.

While the SA process is running, the RS process is operating. The next two capacitors of the array are connected and the voltage reference is split equally between the two capacitors. This is how the reference voltage is scaled in a binary weight fashion by using equally sized capacitors. These two processes continue until all the output bits are obtained. Neglecting non-ideal conditions, the voltage on the comparator input V_{ic} for the i-th step conversion can be expressed as

$$V_{ic} = \frac{1}{i}\left(v_{id} \pm \frac{V_{ref}}{2} \pm \frac{V_{ref}}{4} \pm \cdots \pm \frac{V_{ref}}{2^{i-1}}\right). \tag{1.5}$$

The energy consumed in a complete conversion is expressed as

$$E_{DAC} = C\frac{V_{ref}^2}{2}. \tag{1.6}$$

[2]The capacitance spread is defined as the ratio between the maximum capacitance and the minimum capacitance. As the capacitance spread is reduced, mismatch effects are reduced too.

From (1.6), the power consumption of the DAC is proportional to the unity DAC capacitor and to the square of the reference voltage. Therefore, scaling the technology to reach lower supply voltages and to minimize the capacitor value, allows to reduce the power consumption significantly. The energy consumed by the DAC should not change with the resolution.

Figures 1.12 and 1.13 describe a step-by-step operation for a 4-bit example of a PRS SAR ADC. As the example shows, for a B-bit output, B positive edge of the clock are needed.

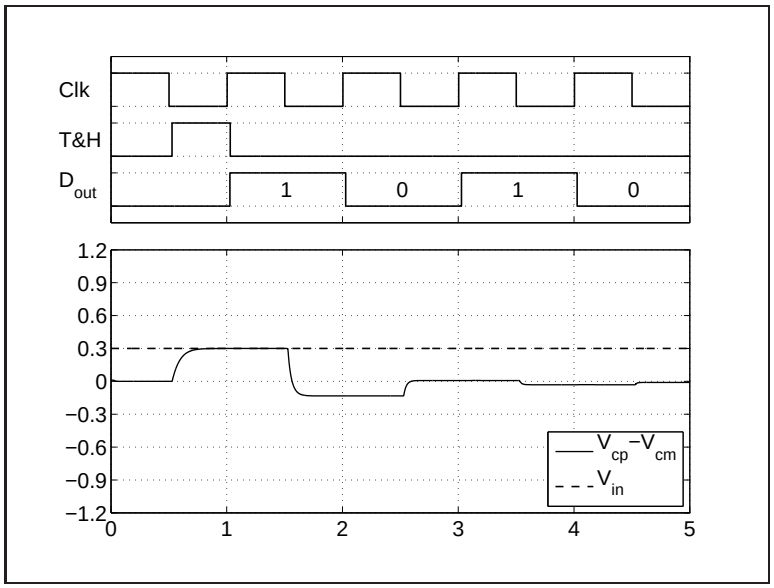


FIGURE 1.12. Simulated comparator input and output for a 4-bit PRS SAR ADC. $V_{in} = 300\ m$V, and $V_{ref} = 1.2$ V.

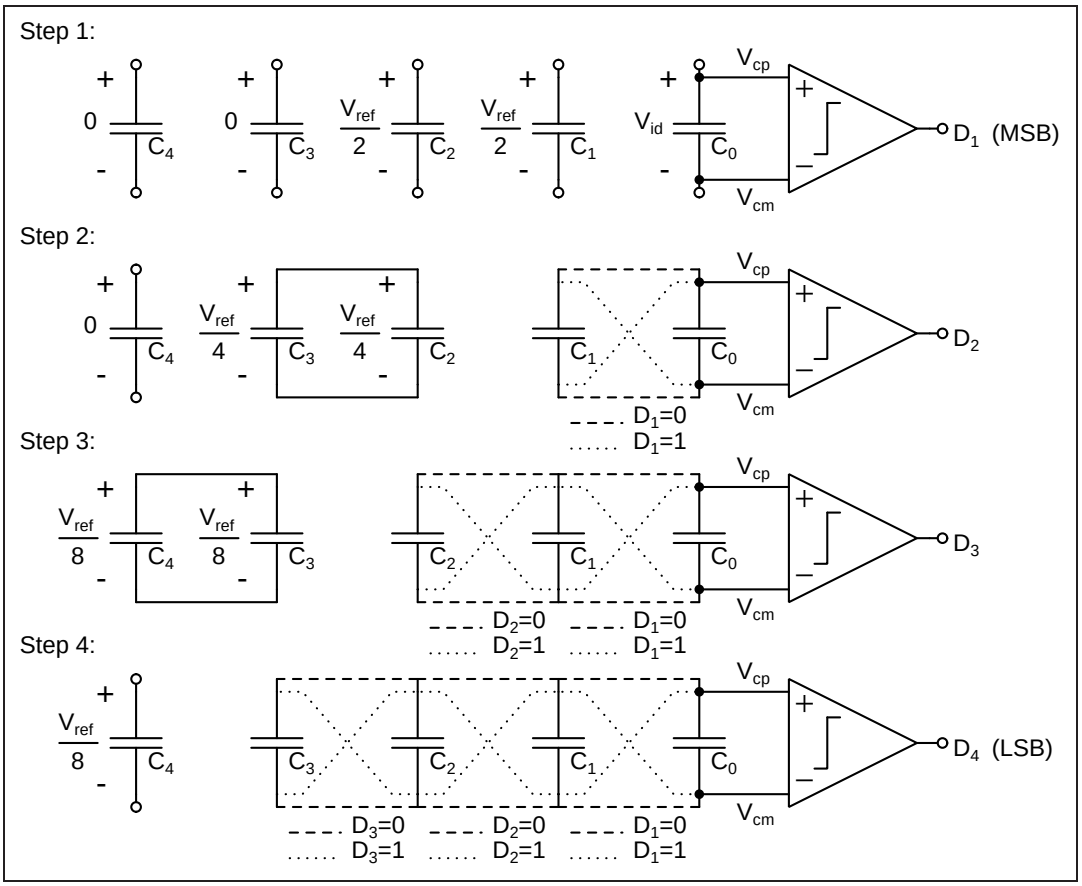


FIGURE 1.13. 4-bit sequence of connection in PRS SAR ADC throughout a conversion.

1.4.1. First Implementation of the PRS SAR ADC.

A first version of the PRS SAR ADC was presented in (Alvarez-Fontecilla & Abusleme, 2015). Table 1.1 shows the performance metrics of the solid-state implementation. The results reveal the energy efficiency of the passive reference sharing algorithm. With a reduced die area, this topology is suitable for biomedical applications, but, the resolution is not enough to reach competitive standards.

TABLE 1.1. Results of the first implementation of the PRS SAR ADC. Total power consumption does not consider the clock generation.

Number of bits (B)	6 bits
Technology process	0.18 μm
Die area	0.0168 mm^2
Total capacitance	700 fF
Clock frequency	12.5 MHz
Sampling frequency (f_s)	1.5625 MS/s
Total power	2.07 μW
DNL	0.912/-0.689 LSB
INL	0.896/-0.611 LSB
SNDR@f_s	33.8 dB
ENOB@f_s	5.17 bits
FoM	30.9 fJ/conv-step

1.5. Thesis Contribution

The main objetive of this work is to evaluate the performance limits of the passive reference-sharing architecture, in order to propose an optimized design of the first version of the PRS SAR ADC, to maintain the low power consumption and increase the bit resolution and the speed. For this, a complete circuit analysis is revised, incorporating the effect of the CMOS switch capacitance, new DAC topologies to increase the operation frequency, asynchronous logic to reduce the digital power consumption and the effects of the dynamic comparator in the global performance. Finally, a solid-state integrated circuit of the proposed solution is built using a 0.13 μm process.

The second objetive of the thesis is to propose a high-performance ADC for ultra low-power applications, such as biomedical sensor nodes, taking advantage of the small die area and the high energy efficient algorithm. The device is expected to reach similar performance metrics as the current state of the art devices.

Finally, together with the ADC optimization, a complete mixed signal design flow is developed and validated for a Globalfoundries 0.13 μm technology, which is part of the academic research program of MOSIS with no fabrication cost.

1.6. Methodology and Thesis Structure

The methodology of the thesis follows a mixed-signal design flow as shown in Figure 1.14. First, according to the specifications, a behavioral analysis is carried out. Second, circuit simulations for the analog part are executed, while for the digital part, synthesis and simulations are done using a hardware description language (HDL) compiler. Third, in a mixed-signal platform, a circuit simulation is performed including the analog schematic and the digital synthesized file. At this stage, the complete circuit operation can be tested in a preliminary version. Fourth, the layout is implemented. For the analog track, LVS (layout versus schematic) and DRC (design rule check) steps are completed to verify a correct implementation of the original schematic and to ensure technology specifications. Then a parasitic extraction is performed to simulate the post-layout analog stage. For the digital track, the layout implementation is accomplished by a place-and-route tool. This tool also includes a DRC step. Then, with the resulting Verilog file, simulation are carried out to validate its functionality. Finally, each track results in a GDS (graphical data system) file. Both files can be imported in to mixed-signal environment to executed again a DRC step, extract parasitic components and simulate the complete chip. Once the operation of the integrated circuit has been verified, it is ready for fabrication.

The thesis structure also follows the design flow. In Chapter 2 an analysis of the PRS SAR ADC is made in order to find the restrictions that limit the performance of the proposed ADC. Then with the theoretical result an optimized design is proposed. In Chapter 3, with a proposed design, the circuit operation and implementation of each block is presented. This chapter ends with the complete ADC layout. In Chapter 4, post simulation results are shown and compared with the first version and with the state of art. Finally, in Chapter 5 conclusion are shown and future work is proposed.

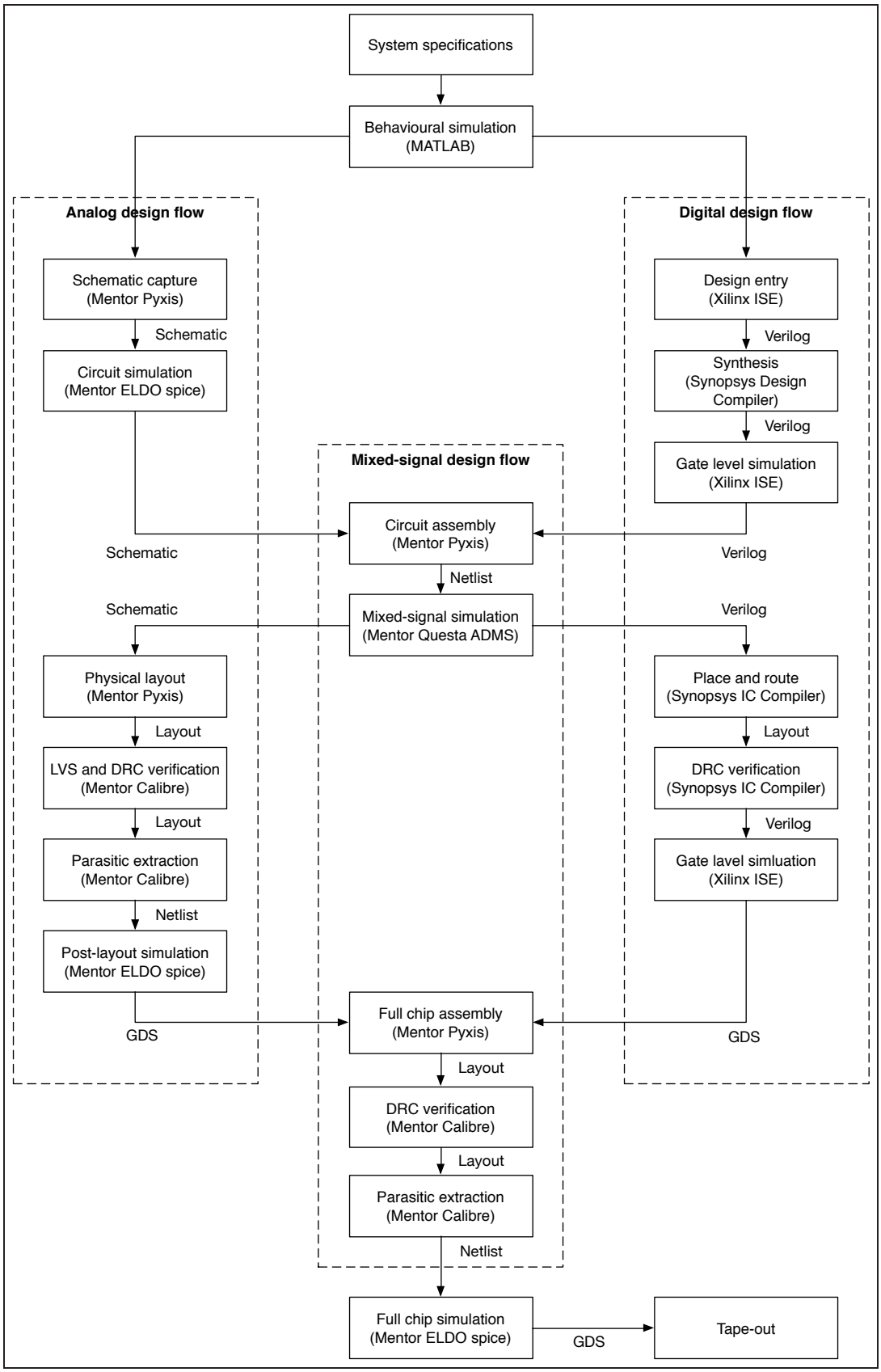


FIGURE 1.14. Mixed signal integrated circuit design flow chart.

2. APPROACHES AND CHALLENGES OF THE PRS SAR ADC

This chapter describes the design-space and the parameters that limits the performance of the PRS SAR ADC. Each of the following topics: parasitic capacitance, noise, DAC multiple RC network and comparator input offset, are described to maximize the resolution, maximize the speed, reduce non-linearities values, and estimate the best value for the unity DAC capacitance with the aim to minimize the DAC power consumption.

2.1. Parasitic Effects on Passive Sharing Process

In a solid-state implementation, parasitic components cannot be avoided. The PRS SAR ADC operates in the charge domain, hence any charge loss or change in the DAC array capacitor will degrade its performance. Then, it is relevant to find the effect of the parasitic capacitance at the layout implementation, as well as the intrinsic capacitance of the CMOS switches used for the passive charge-sharing process.

2.1.1. CMOS Switch Parasitic Components

Figure 2.1 shows the equivalent circuit of a CMOS switch. In a saturation region, the components expression are (Razavi, 2000)

$$C_{gs,np} = C_{gd,np} = \frac{1}{2} W_{np} L C_{ox} + C_{ol} \tag{2.1}$$

$$C_{gg,np} \approx (C_{gs,np} + C_{gd,np}) \tag{2.2}$$

$$r_{ds,np} = \frac{1}{\mu_{np} C_{ox} \dfrac{W_{np}}{L} (|V_{gs,np}| - |V_{t,np}|)} \tag{2.3}$$

where the np subscript stand for a NMOS or PMOS transistor, and C_{ol} correspond to the overlap capacitance. To analyze the effect of the parasitic component in the charge domain, only the switch capacitance are considered. To describe the ratio between the unity DAC capacitor and the CMOS switch contribution, a β factor is defined as

$$\beta = \frac{C_{gg,p} + C_{gg.n}}{C}. \tag{2.4}$$

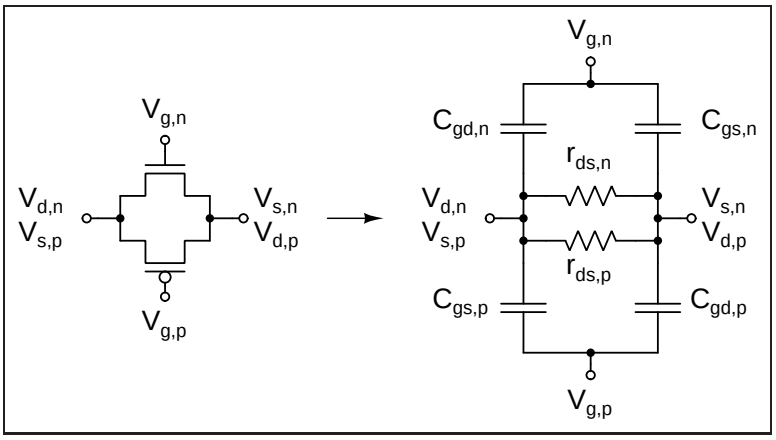


FIGURE 2.1. CMOS switch equivalent circuit.

2.1.2. Layout Parasitic Capacitance Assumptions

The parasitic capacitance elements arising from the implementation of the DAC capacitor array depends on the layout. As proposed in (Alvarez-Fontecilla & Abusleme, 2015), to simplify the parasitic effects analysis, it is assumed that the unity capacitors are aligned in a straight line and the connections between them are symmetrical. The equivalent circuit between two adjacent elements is shown in Figure 2.2, where the r, l, b, t and m subscripts stand for right, left, bottom, top and middle. The middle capacitors correspond to the unity DAC capacitors, defined as

$$C_{ml} = C_{mr} = C. \tag{2.5}$$

To describe the ratio between the unity DAC capacitance and the layout parasitics, factor α and γ are defined for the ground and cross parasitic components, respectively. Assuming a symmetrical implementation, α and γ are defined as

$$\alpha = \frac{C_{tl}}{C} = \frac{C_{tr}}{C} = \frac{C_{bl}}{C} = \frac{C_{br}}{C} \tag{2.6}$$

$$\gamma = \frac{C_{rl}}{C} = \frac{C_{lr}}{C} = \frac{C_{bt}}{C} = \frac{C_{tb}}{C}. \tag{2.7}$$

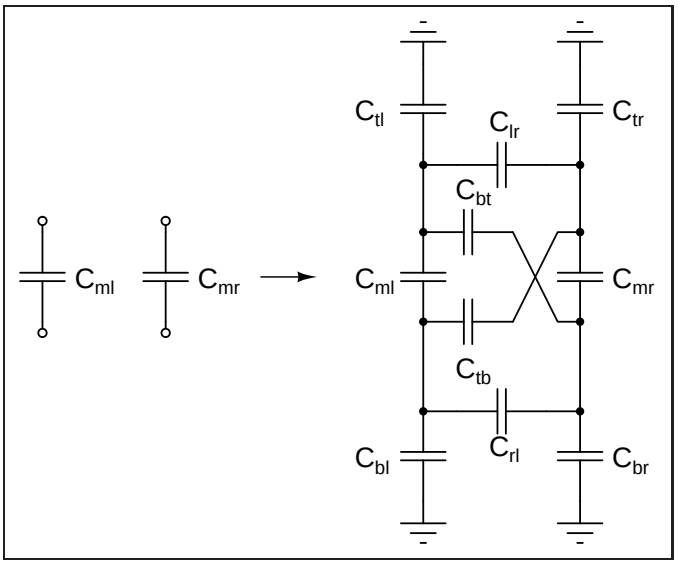


FIGURE 2.2. A fraction of the capacitive DAC array equivalent circuit.

2.1.3. Passive Charge-Sharing Process Analysis

The goal of this analysis is to mesure the variation of voltage in the unity DAC capacitor labeled with the m subscript. In Figure 2.3 the process of passive charge sharing including the layout and CMOS switch capacitive elements is shown, where the left and right equivalent circuit are before and after the charge-sharing process.

As explained in the Appendix A, there is an equivalence between a series and parallel passive charge sharing. Figure 2.4 describes the process in a parallel equivalent circuit. This analysis is only valid for a direct connection between the DAC capacitors, however the cross connection is analogous. Thus, the initial and final charge in the capacitors between the V_m nodes is

$$Q_{m,i} = (C_{tl} \parallel C_{bl} + C_{tb} + C_{ml})V_{ml} + (C_{tr} \parallel C_{br} + C_{bt} + C_{mr})V_{mr} \tag{2.8}$$

$$Q_{m,f} = C_m V_m \tag{2.9}$$

where C_m is the equivalent capacitance defined as

$$C_m = C_{tl} \parallel C_{bl} + C_{tb} + C_{ml} + C_{tr} \parallel C_{br} + C_{bt} + C_{mr} + C_{gg,p} \parallel C_{gg,p} + C_{gg,n} \parallel C_{gg,n}. \quad (2.10)$$

Equating the charge expressions (2.8) and (2.9), the final voltage V_m is written as

$$V_m = \frac{(C_{tl} \parallel C_{bl} + C_{tb} + C_{ml})V_{ml} + (C_{tr} \parallel C_{br} + C_{bt}. + C_{mr})V_{mr}}{C_m}. \quad (2.11)$$

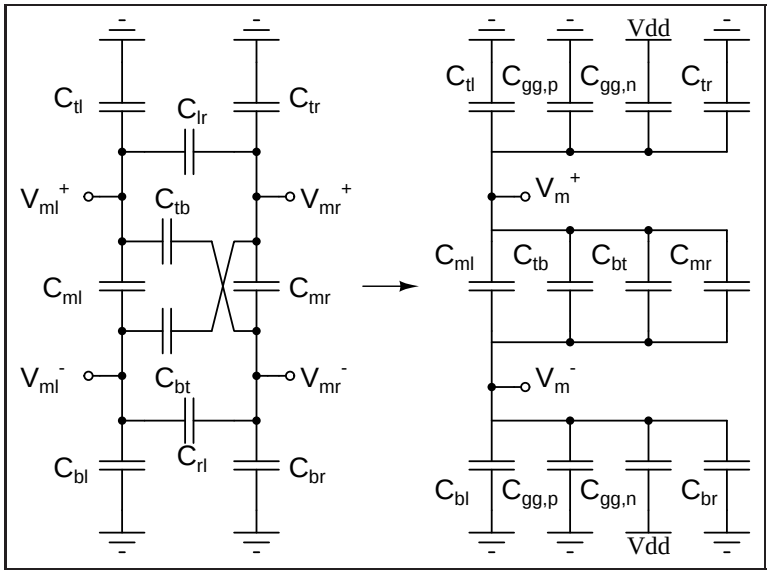


FIGURE 2.3. Equivalent circuit of the capacitive DAC array.

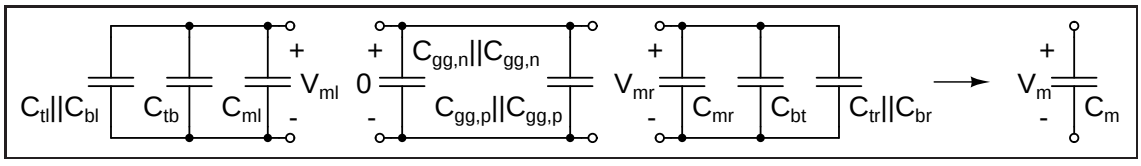


FIGURE 2.4. Equivalent circuit of the parallel-connected capacitive DAC array.

2.1.4. Parasitic Effects in the Successive Approximation Process

In the successive approximation process, for each conversion step a new capacitance is connected to the DAC array. Thus, the value of the rightmost branch of Figure 2.3 must consider the previous capacitors. Therefore, for the i-th conversion, and $i \geq 2$, the rightmost branch capacitors are redefined as

$$C_{mr} = (i-1)C + 2(i-2)\gamma C \tag{2.12}$$

$$C_{tr} = C_{br} = (i-1)\alpha C + (i-2)\beta C. \tag{2.13}$$

Considering the definitions (2.4), (2.5), (2.6) and (2.7), the equivalent capacitance after the sharing process is expressed as

$$C_m = C\left(i\left(1+\frac{\alpha}{2}\right) + 2(i-1)\gamma + (i-1)\frac{\beta}{2}\right) \tag{2.14}$$

Then, replacing the capacitor values in (2.11), the voltage in the comparator after the i-th step conversion, for $i \geq 2$, can be expressed as

$$V_c = V_{ml}h(\alpha,\beta,\gamma,i) + V_{mr}\left(1 - h(\alpha,\beta,\gamma,i)\right) \tag{2.15}$$

where,

$$h(\alpha,\beta,\gamma,i) = \frac{\dfrac{\alpha}{2}+\gamma+1}{i\left(1+\dfrac{\alpha}{2}\right) + 2(i-1)\gamma + (i-1)\dfrac{\beta}{2}}. \tag{2.16}$$

Two important conclusions arise from (2.16). It can be shown that if $\gamma = \beta = 0$ and $\alpha \neq 0$, the result is equivalent to the ideal case. Therefore, the parasitic capacitance connected to ground does not degrade the charge sharing process. On the other hand, if $\alpha \gg \gamma$ and $\alpha \gg \beta$, the voltage on the comparator reaches its ideal value, so bigger ground capacitances mitigate the effect of cross and switch capacitances.

2.1.5. Parasitic Effects in the Reference Sharing Process

In a reference sharing process, in contrast to the successive approximation process, only two of the DAC capacitors interact with each other and after the charge is shared the switches are opened. Before the sharing process, one capacitor stores a cero voltage value, and the other, a value corresponding to the actual i-th conversion step. Thus for $i \geq 2$, the initial voltage on each capacitor shown in Figure 2.3 is defined as

$$V_{ml} = 0 \tag{2.17}$$

$$V_{mr} = \frac{V_{ref}}{2^i} \tag{2.18}$$

Then, considering the definitions (2.4), (2.5), (2.6) and (2.7), the equivalent capacitance after the sharing process can be expressed as

$$C_m = C\left(\alpha + 2\gamma + 2 + \frac{\beta}{2}\right) \tag{2.19}$$

Therefore, replacing the capacitor values for this case in (2.11), the resulting voltage and charge of the first stage are

$$V_{rs,0} = \frac{V_{ref}}{2^i}\left(\frac{1}{2} - \frac{\beta}{4\alpha + 8\gamma + 8 + 2\beta}\right) \tag{2.20}$$

$$Q_{rs,0} = V_{rs,0}\left(\alpha + 2\gamma + 2 + \frac{\beta}{2}\right)C \tag{2.21}$$

From equation (2.20), it can be shown that if $\beta = 0$, $\alpha \neq 0$ and $\gamma \neq 0$, the result voltage is equal to the ideal case. Therefore, parasitic capacitances due to layout implementation do not affect the reference sharing process. During aperture of the switches, the charge in each capacitor is given by

$$Q_{rs,f} = V_{rs}\left(\alpha + 2\gamma + 2\right)C \tag{2.22}$$

Using the charge expression in (2.21) and (2.22), during the i-th conversion step, the final voltage on each capacitor is obtained as

$$V_{rs} = \frac{V_{ref}}{2^{(i+1)}}. \tag{2.23}$$

Equation (2.23) shows that the parasitic capacitances of the switches do not affect the final voltage. Therefore, the parasitic elements do not degrade in any form the passive reference sharing process.

2.1.6. Limitations due to Parasitic Capacitance

From the analysis above, only the successive approximation process is affected by the parasitic capacitive elements, and only the cross and switch parasitic capacitances leads to a voltage difference in the comparator input. To measure the impact of these components, the maximum values of β and γ are obtained to achieve linearities requirements for different number of bits B. The maximum values for the γ factor are shown in Figure 2.5.

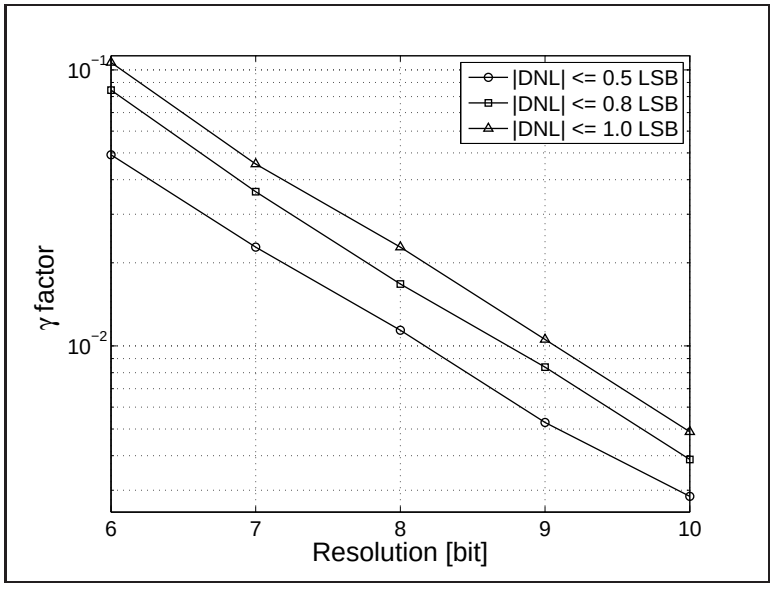


FIGURE 2.5. Cross parasitic to unity DAC capacitance ratio γ required to achieve a linearity specification for a number of bits B.

While the real value of the γ factor depends on the layout design and can be reduced by a well-oriented floorplan, the minimum switch capacitance is limited by the minimum size of the CMOS switch implementation. Thus, there is a limitation of the minimum size of the unitary DAC capacitance in order to reach a β that do not result in missing codes. In Figures 2.6 and 2.7 the maximum β factor and minimum unity DAC capacitance are shown for different number of resolution bits.

2.2. Noise Analysis

In a PRS SAR ADC there are three main noise sources: The switching of the reference sharing and sampling process, the RC network of the successive approximation process, and the dynamic comparator.

In this section the noise sources are estimated to obtain their effect on the ADC performance. The analysis in this section is heavily based on the previous works of the PRS SAR ADC by (Alvarez-Fontecilla & Abusleme, 2015).

2.2.1. Noise due to the reference sharing and sampling processes

In a sampling process, the on-resistance of a switch introduces a thermal noise in the system. The total integrated noise in the hold capacitor after the hold process finishes is given by the "well known" expression KT/C (Pelgrom, 2010), which in the voltage domain is given by $\sqrt{kT/C}$, where k is the Boltzmann constant, T the switched absolute temperature and C the hold capacitor value.

In a PRS SAR ADC, after the track-and-hold process, each capacitor of the DAC array holds a voltage noise power of kT/C. Then, during the reference-sharing process the DAC capacitors share the noise contribution of the sampling process and also increase the thermal noise due to the commutation process itself. Finally the total contribution of this process is the sum of all the voltage noise powers on each i-th capacitor. Therefore, the

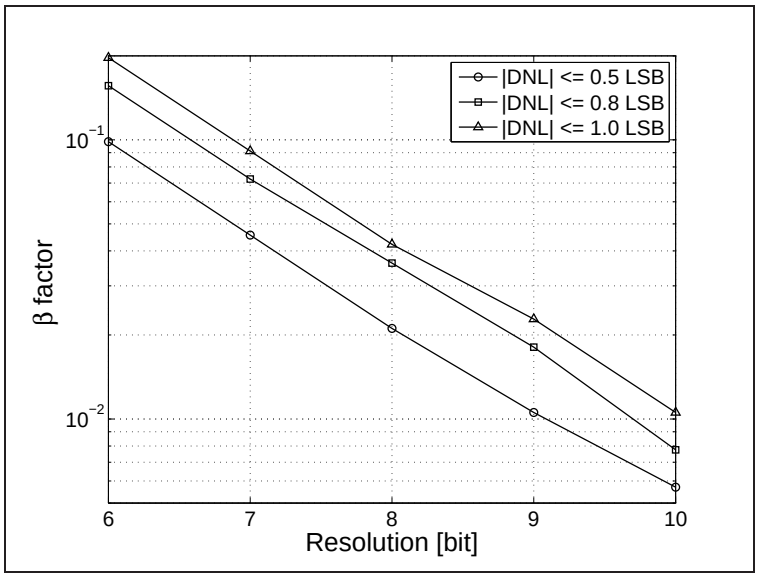


FIGURE 2.6. CMOS parasitic capacitance to unity DAC capacitance ratio β required to achieve a linearity specification for a number of bits B

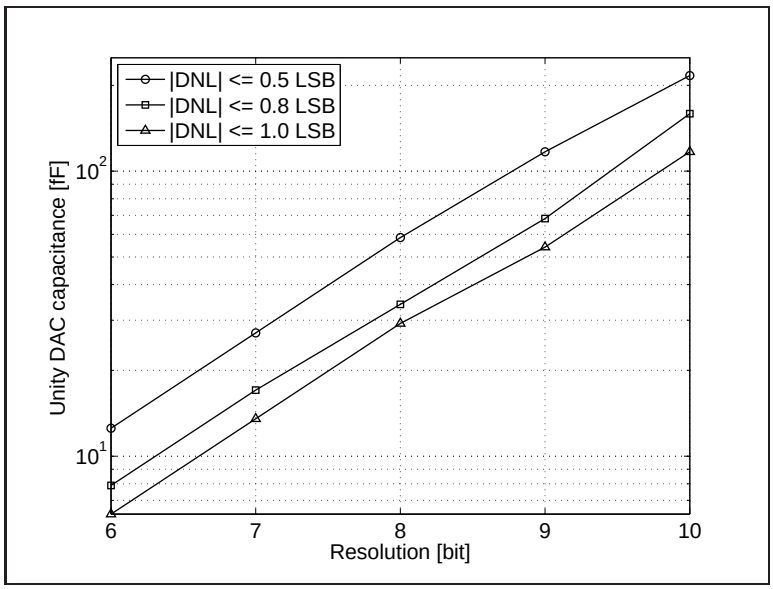


FIGURE 2.7. Minimum unity DAC capacitance required to achieve a certain linearity specification, when using a minimum switch capacitor size for 130 nm fabrication process and a given number of bits B.

noise contribution of the reference sharing and sampling process can be computed as

$$\overline{v_{n1}^2} = \sum_{i=0}^{B-1} \overline{v_{nC_i}^2} = f(B)\frac{KT}{C} \tag{2.24}$$

where $f(B)$ is a noise factor that depends on the resolution. In order to obtain a numerical value to use in further analysis, it is assumed that the noise sources of the same capacitor or switching process are fully correlated, which correspond to the worst case. An example for a 4-bit ADC is detailed in Appendix B.

2.2.2. Noise due to the Successive Approximation Process

During the charge sharing in the successive approximation process, an RC network is added on each new step. For an RC network the total integrated noise is obtained by the Nyquist theorem for passive RLC circuits (Enz & Vittoz, 2006).

$$\overline{V_n^2} = kT\left(\frac{1}{C_\infty} - \frac{1}{C_0}\right) \tag{2.25}$$

where C_∞ correspond to the capacitance seen by the involved port when the real part of the impedance is an open circuit, and C_0 when real part of the impedance is a short circuit.

Using (2.25), and assuming that the RC network of the DAC is composed only by the switch resistance and the DAC unity capacitance, the total integrated noise contribution in the successive approximation process is

$$\overline{v_{n2}^2} = B^2\left(1 - \frac{1}{B}\right)\frac{kT}{C} \tag{2.26}$$

The attenuation factor B^2 is for the passive charge-sharing process itself, indicated in equation (1.5). The expression (2.26) is valid for any of the DAC architecture that will be discussed in Section 2.3.

2.2.3. Noise due to the Dynamic Comparator

Dynamic comparators do not have a DC current, making it difficult to compute the input-referred noise analytically. In the literature there are no closed-form expressions to

analyze the noise of a latched comparator. In (Nuzzo, De Bernardinis, Terreni, & Van der Plas, 2008) there is an analysis that yields a width ratio of the input and tail transistors in order to minimize the input-referred noise. Even though this rule can be considered in the comparator design, it does not predict the resulting input-referred noise.

In general, the noise contribution of the comparator, considering the attenuation of the signal showed in (1.5), is defined as

$$\overline{v_{n3}^2} = B^2\overline{v_{ncomp}^2}. \tag{2.27}$$

2.2.4. Limitations due to the Noise Contributions

Considering all the noise contribution, the total integrated noise at the input of the comparator as a function of the resolution can be expressed as

$$\overline{v_n^2} = \left(f(B) + B^2\left(1 - \frac{1}{B}\right)\right)\frac{KT}{C} + B^2\overline{v_{ncomp}^2} \tag{2.28}$$

The comparator noise contribution is not relevant to to obtain a limit value of the DAC capacitor size. Therefore, (2.28) can be rearranged as:

$$\overline{v_n^2} = g(B)\frac{kT}{C} \tag{2.29}$$

where,

$$g(B) = f(B) + B^2\left(1 - \frac{1}{B}\right). \tag{2.30}$$

Using (2.30), the numerical value of $g(B)$ can be obtained using scientific computation software and the results are shown in Figure 2.8. It reveals how the noise contribution factor $g(B)$ increases significantly with the resolution.

As an example, considering a noise design requirement of $\overline{v_n^2} \leq (LSB/2)^2$ and a voltage reference of 1.2 V, the minimum values of the unit capacitor of the DAC for a given resolution are shown in Figure 2.9. The noise introduces a limitation on the power consumption of the DAC array, due to the restricted capacitor size. It is important to note that the maximum resolution is limited by the die area occupied by large capacitors.

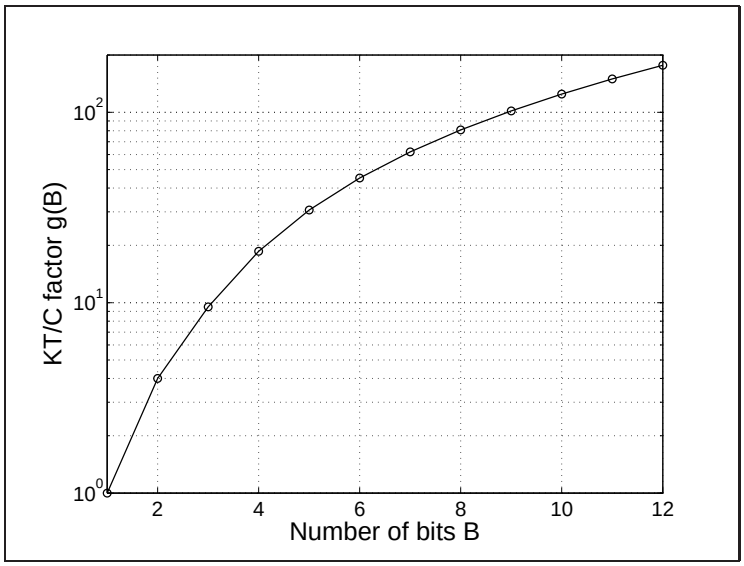


FIGURE 2.8. kT/C factor as a function of the resolution B.

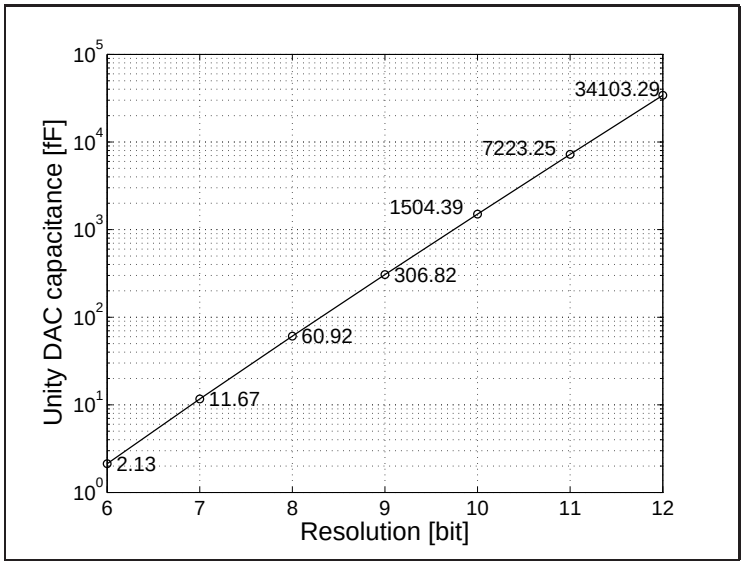


FIGURE 2.9. Minimum capacitor size of the DAC array as a function of the resolution B, considering $V_{ref} = 1.2$ V and $\overline{v_n^2} \leq (LSB/2)^2$.

2.3. Time Response Analysis for Multiple RC Networks

In SAR architectures, the RC network of the DAC array always limits the speed, since it is slower than the dynamic comparator and the digital logic. However, in ultra low-power applications, speed is not a relevant aspect to optimize. Anyway, it is interesting to analyze the time response of a passive charge-sharing process to estimate the maximum operating frequency and to explore new architectures of the DAC array to increase the speed. In this section, two types of DAC architecture are analysed. The first one is based on the design implemented in (Alvarez-Fontecilla & Abusleme, 2015), and the second one is designed to reach a shorter settling time. Both of the proposed DAC architectures are coherent with the parasitic capacitance and noise analysis previously presented.

To simplify the analysis, the RC network only considers the resistance of the CMOS switch and the unity DAC capacitors, the parasitic capacitance are neglected. Also, all the analysis in this section used an equivalent half-circuit of the differential DAC array.

2.3.1. Time Response Comparison on Multiples RC Networks

In multiple RC network with passive sharing it is difficult to obtain a close-form expression for the settling time, even if it is posible to find the system of linear differential equations and to solve it. To overcome this problem, an open-circuit time constant (Gray, 2009) analysis is used to compare the two proposed DAC architectures.

The open-circuit time constant analysis estimates the dominant time constant of the system as the sum of the time constant for each capacitor, computed from the passive network seen when all the other capacitors are removed. This approach will be used to obtain an equivalent time constant of the last charge sharing process in the conversion, which correspond to the worst case.

2.3.2. Cascade DAC Architecture

A preliminary DAC array is shown in Figure 2.10. This design is based on the implementation by (Alvarez-Fontecilla & Abusleme, 2015). The equivalent half-circuit is shown in Figure 2.11 assuming only direct switch connections.

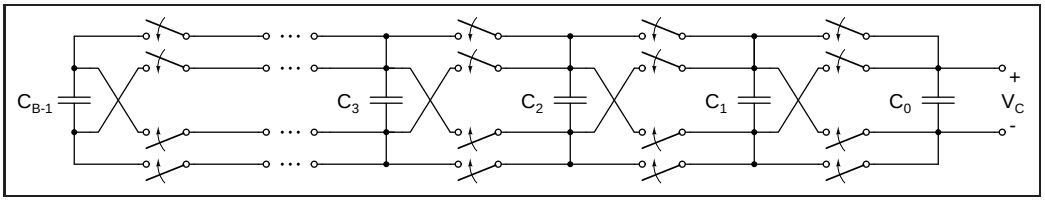


FIGURE 2.10. Cascade DAC architecture.

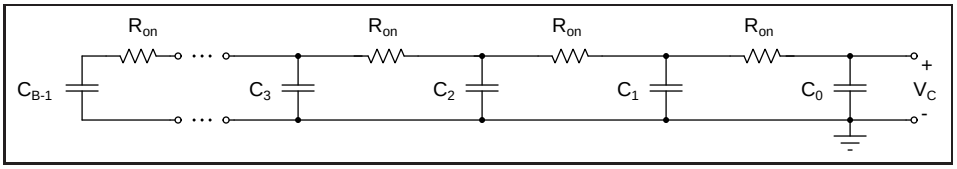


FIGURE 2.11. Equivalent half-circuit for cascade DAC architecture.

From Figure 2.11 and using an open circuit time constant approach, the time constant for the last sharing process is $\tau_1 = RC(B-1)$, for a B-bit resolution.

2.3.3. Two-rail DAC Architecture

A preliminary DAC array is shown in Figure 2.12 for fastest voltage settlings. The equivalent half-circuit is shown in Figure 2.13 assuming only direct switch connections.

From Figure 2.13 and using a open circuit time constant approach, the time constant for the last sharing process is $\tau_2 = RC$, for a B-bits resolusion.

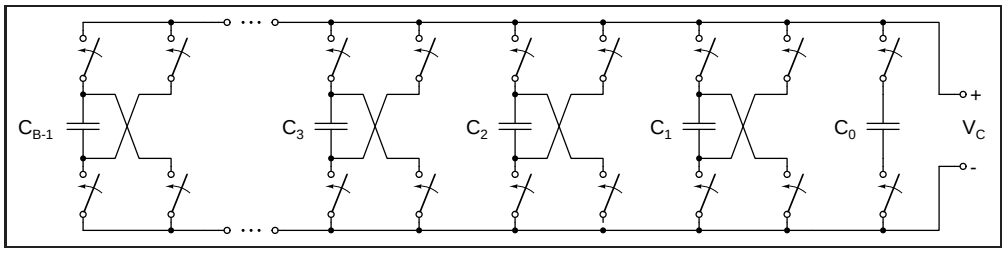


FIGURE 2.12. Two-rail DAC architecture.

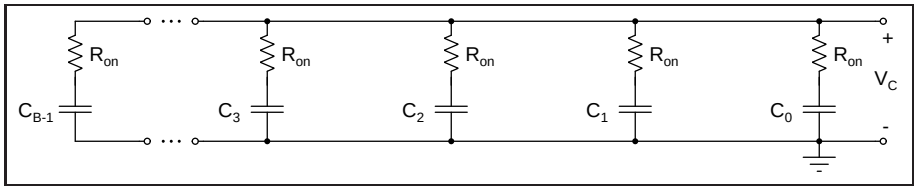


FIGURE 2.13. Equivalent half-circuit for two-rail DAC architecture.

2.3.4. Speed Limitation due to RC Networks

From the expression of τ_1 and τ_2, it is clear that the two-rail architecture is significantly faster than the cascade architecture. To visualize the difference between the two architectures, the solution of the linear differential equations describing each circuit are plotted in Figure 2.14 for $B = 8$ and fixed values of R and C.

No matter which DAC architecture is used, there is a speed limitation due to the on-switch resistance and the DAC capacitors values. According to (2.3) and (2.2), the equivalent on-switch resistance is inversely proporcional to the switch capacitor size, hence if the switch capacitance is minimized in order to minimize the size of the DAC capacitance, the on-switch resistance reaches its maximum value. Then, the fastest settling time is determined by technology limitations and cannot be reduced indefinitely. However, time interleaving techniques may be used to increase the speed.

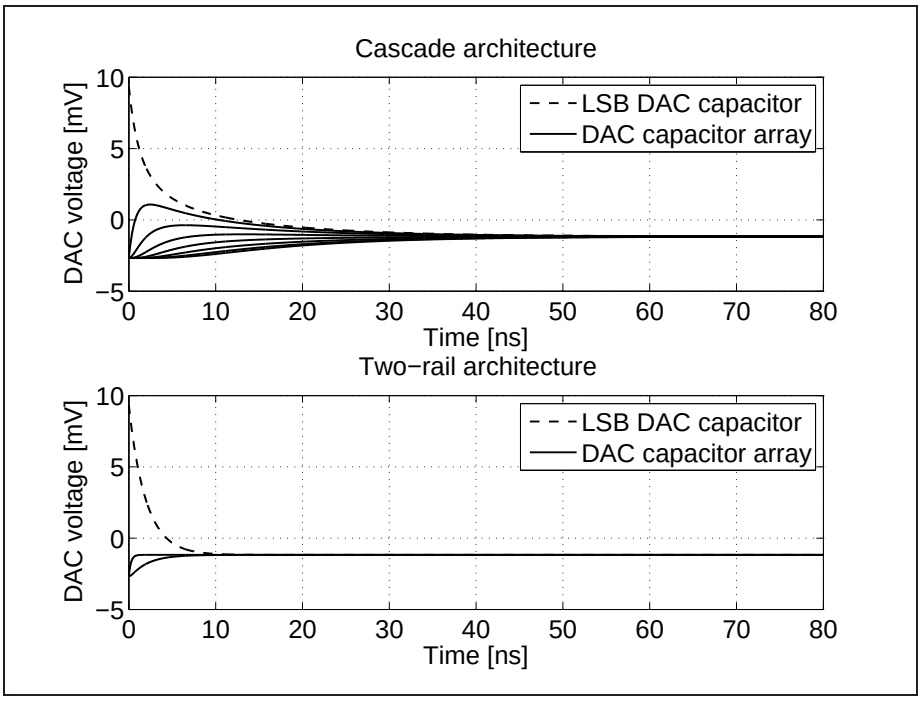


FIGURE 2.14. Settling time comparison between a cascade and two-rail DAC architectures for B=8, R=10 kΩ and C=100 fF.

2.3.5. Time Interleaving Techniques for a PRS SAR ADC

To increase the speed ADCs, time interleaved techniques (J. Black W.C. & Hodges, 1980) may be used. This method consist basically in the use of an array of N converters with an N-phase non-overlapping clocks to increase the sampling frequency by N. The advantages of using time interleaving converters, besides of the inherent speed increase, is the reduction of power. When a single converter reach the operation limit, the power-speed trade off becomes non-linear, increasing the speed in a certain amount, makes the power consumption to increases in a higher value (Razavi, 2013). The drawback of using time interleaving techniques, is the need to overcome the mismatch between the different channels and also generate multi-phase clocks with high timing performance.

As mentioned earlier, the PRS speed is limited by the RC network of the DAC. Other speed constraints are the track-and-hold circuit and the comparator. In the case of the

track-and-hold circuit, an acquisition time is required to ensure an acceptable error. Using a first-order MOS switch model, the tracked voltage in the capacitor can be expressed as

$$V_C(t) = V_{\mathrm{FSR}}(1 - e^{-\frac{2t}{RC}}) \tag{2.31}$$

where R and C correspond to the on switch resistance and the unity DAC capacitance. The factor of 2 in the exponential term is to consider the differential architecture of the design. For an error below half an LSB, the following settling time condition must be met before the hold phase begins

$$t_{hold} \geq \frac{RC}{2} \ln(2^{B+1}). \tag{2.32}$$

For practical values $R = 14\ k\Omega$, $C = 100\ f$F and $B = 8$, the minimum track time is close to 5 ns. This value is higher than the comparator maximum decision time (around 3 ns), therefore the track-and-hold settling time sets the limitation for the maximum value of N channels for an interleaved array. Using $R = 14\ k\Omega$ and $C = 100\ f$F for the on resistance and DAC capacitors components, a valid value for the clock period is 40 ns. With this value in a single converter, a maximum speed of 3.125 MS/s is reached. The division between the semi-period of the clock cycle with the track acquisition time gives the maximum number of channels. In this case, a maximum of 4 channels could be posible. Therefore, the speed of the PRS SAR ADC can be increased by 4 to a value of 12.5 MS/s.

2.4. Performance Degradation by the Comparator Offset

Considering the input offset voltage of the comparator, V_{os}, equation (1.5) can be re-defined as

$$v_c(i) = \frac{1}{i}\left(v_{id} \pm \frac{V_{ref}}{2} \pm \frac{V_{ref}}{4} \pm \cdots \pm \frac{V_{ref}}{2^{i-1}}\right) + V_{os}. \tag{2.33}$$

Equation (2.33) shows how sensitive the PRS SAR ADC is to the comparator input offset. Using computer calculations, the maximum acceptable comparator offset to avoid missing codes can be obtained as a function of the resolution. The result is shown in Figure 2.15. It indicates how the comparator offset sets a limitation on the resolution, because even if a calibration system is used, offset values less than 1 mV are not posible.

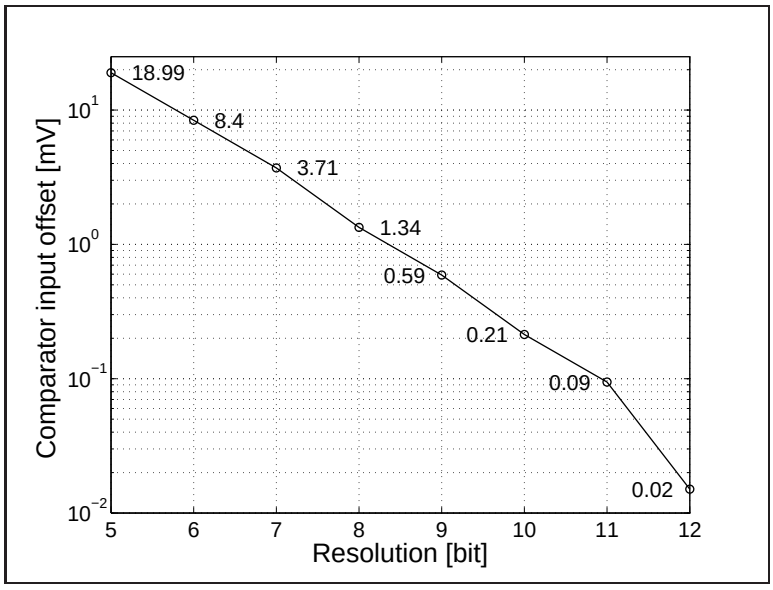


FIGURE 2.15. Maximum comparator input voltage offset to avoid missing codes ($|\mathrm{DNL}| \leq 1$) for a given number of bits B.

2.5. Resolution, Frequency and Power Consumption Limitations

In this chapter, four design parameters of the PRS SAR ADC are described to increase the resolution, minimize the DAC power consumption, increase the speed and achieve linearity requirement. In Table 2.1 the effect of each design parameters is summarized, indicating which performance metric is affected.

TABLE 2.1. Performance limiting factors of the PRS SAR ADC.

Design parameter	Limitation
Total integrated noise	Minimum DAC power consumption
Parasitic capacitance	Minimum DAC power consumption and linearity
Comparator input offset	Maximum resolution and linearity
DAC RC network	Maximum sample frequency

In order to maximize the resolution of the ADC, the comparator input voltage imposes a limitation. It can be concluded that a resolution higher than 8 bits is not practical for a solid-state implementation, because the minimum comparator offset voltage to avoid missing codes cannot be reached.

Respect the DAC power consumption, the unity DAC capacitor size is limited due to the non-linearities introduced by the parasitic capacitive elements and noise considerations. For an 8-bit and 1.2 V ADC, the minimum capacitor size is entirely limited by noise requirements, giving a minimum value of 60 fF.

Finally, considering a minimum sized switch, the minimum settling time for the passive charge-sharing process in the DAC is close to 10 ns. Then, a maximum clock frequency is 50 MHz. From this, and considering a 8-bit converter, the maximum sampling frequency is 6.25 MS/s.

From the above, a 8-bit ADC is proposed, constructed with a 100-fF unity capacitor for the DAC array. The unity capacitor value is selected higher than the minimum value in order to reduce the effect of CMOS parasitic capacitance and to tolerate better the layout cross parasitic capacitance. In Table 2.2 the preliminary characteristics of the ADC are presented.

TABLE 2.2. Proposed design for an optimized PRS SAR ADC.

Stated resolution	8-bit
Unity DAC capactance value	100 fF
Total capacitance	900 fF
DAC architecture	Two-rail architecture
CMOS switch size	Minimum
Maximum clock frequency	33.33 MHz
Maximum sampling frequency	4.17 MS/s

3. DESIGN AND IMPLEMENTATION OF THE PRS SAR ADC

This chapter describes the complete circuit design and implementation of the PRS SAR ADC. On each circuit block the design is explained in term of its operation and design considerations. Also, the layout implementation is detailed in order to accomplish the assumptions made in previous chapters.

3.1. Technology Description

The technology process used for the solid-state implementation of the PRS SAR ADC is Globalfoundries 0.13 μm 8RF-DM.

This technology process is part of the MOSIS academic research program (MOSIS, 2015). The mixed-signal design kit (PDK) of this technology is available for Mentor Graphics EDA tool. Also an ARM standard library is available, enabling synthesis of place-and-route digital design flow, which its supported by Synopsys Design and IC Compiler.

3.2. DAC Capacitor Array

The circuit implementation of the DAC capacitor array is shown in Figure 3.1 and corresponds to a two-rail architecture for an 8-bit resolution. The RS and SA suffix in the switches are for the reference sharing and successive approximation process.

3.2.1. Circuit Design

The DAC array has two main components, the unity capacitor and the CMOS switches. A standard cell is designed, containing one metal-over-metal (MOM) capacitor, four CMOS switches at the top and other four CMOS switches at the bottom. To achieve a symmetrical layout, this cell is replicated one next to the other, to finally construct the complete DAC array. Although, the first and last capacitors of the array have a different structure, the same standard cell is used to ensure that every capacitor has the same parasitic components.

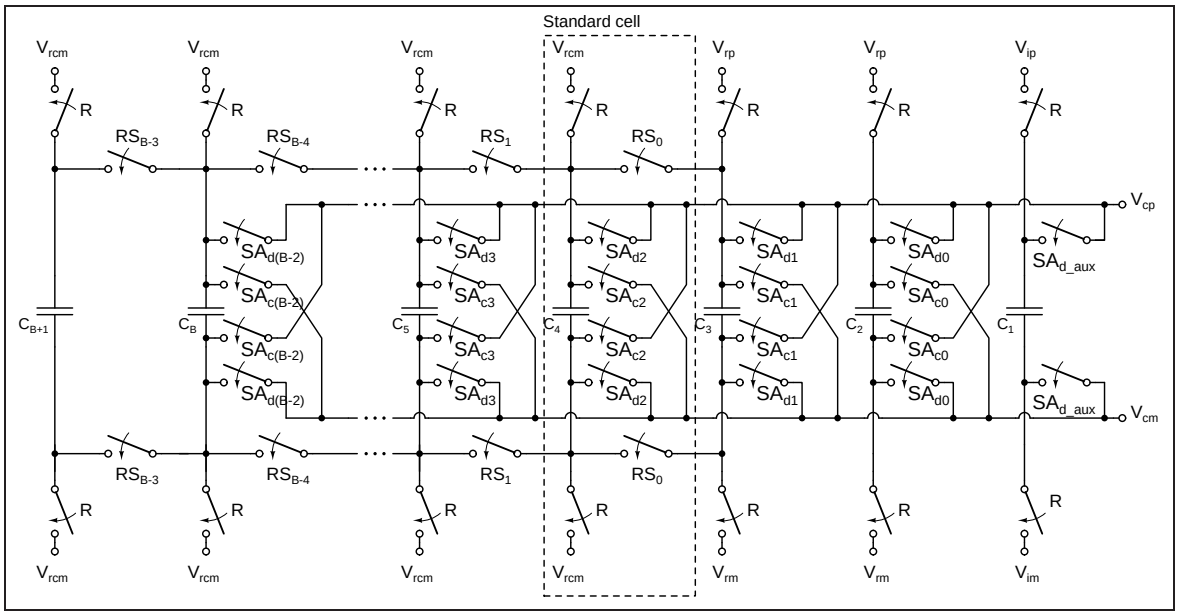


FIGURE 3.1. DAC capacitor array schematic for a B bit implementation.

3.2.1.1. Capacitor Charaterization

For the Globalfoundries 0.13 μm technology a vertical natural capacitor (IBM, 2010) is available with the respective statistical information. This type of MOM capacitor is symmetrical and can be stacked using three types of metal to increase the capacitance. Figure 3.2 describes the shape of the MOM capacitor.

With the statistical data, a Monte Carlo (MC) simulations can be carried to to ensure that the mismatch variation does not decrease the ADC performance. In Figure 3.3 the INL and DNL are shown for a MC simulation for a 100-fF capacitor and an 8-bit implementation. The result indicates that there are no missing codes.

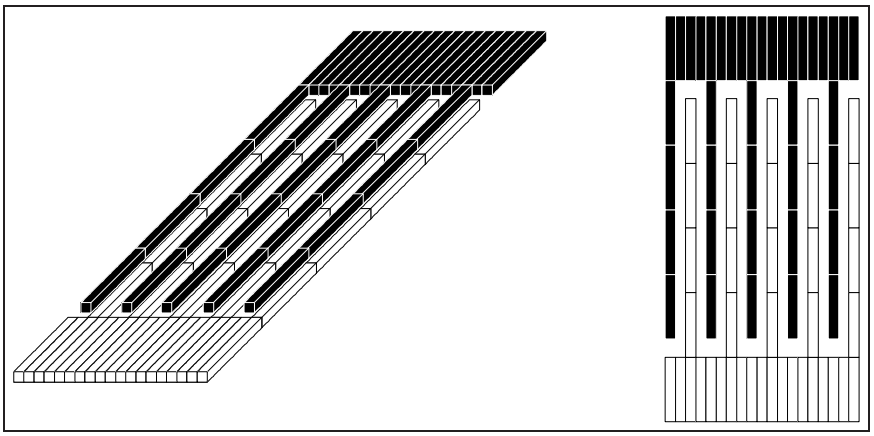
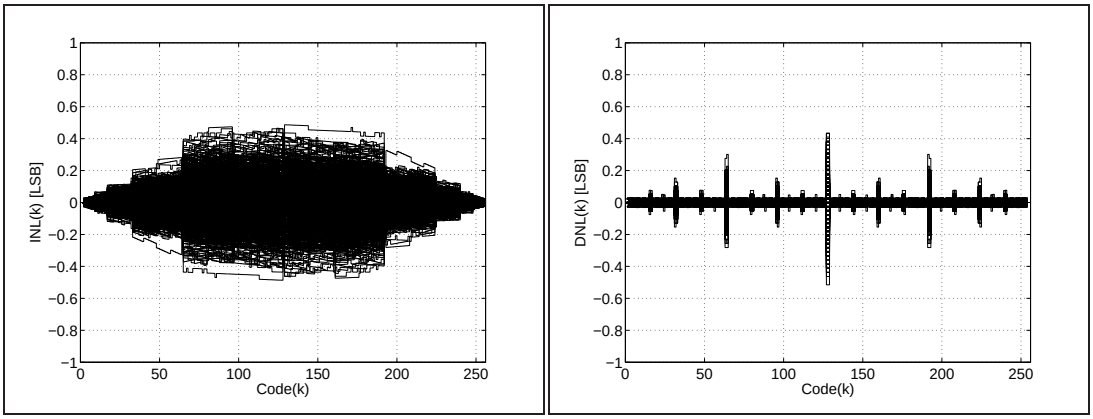


FIGURE 3.2. Vertical natural capacitor for one metal layer.



(a) Integral non-linearity (INL). (b) Differential non-linearity (DNL).

FIGURE 3.3. Mismatch effects of vertical natural capacitor for 1000 iterations of a 8 bits ADC with an unitary DAC capacitor size of 12.28 $\times$ 20 mm^2 (100 fF).

3.2.1.2. CMOS Switches Characterization

The circuit implementation of the CMOS switch is shown in Figure 3.4. Table 3.1 indicates the transistor sizes.

To minimize the on-resistance a ratio of $M_3/M_4 = 3$ must be considered. Figure 3.5 is a simulation result that describes the resistance variation for all the voltage range when the switch is closed.

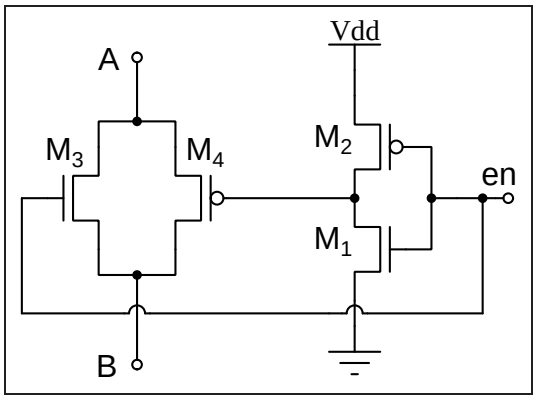


FIGURE 3.4. CMOS switch schematic. For transistor M_3 and M_4 the bulk is connected to ground and $V_{\rm dd}$, respectively.

TABLE 3.1. CMOS switch transistors size. For all transistors $L = 0.12$ μm.

Transistor	Width [μm]	Transistor	Width [μm]
M_1	0.16	M_3	0.16
M_2	0.32	M_4	0.48

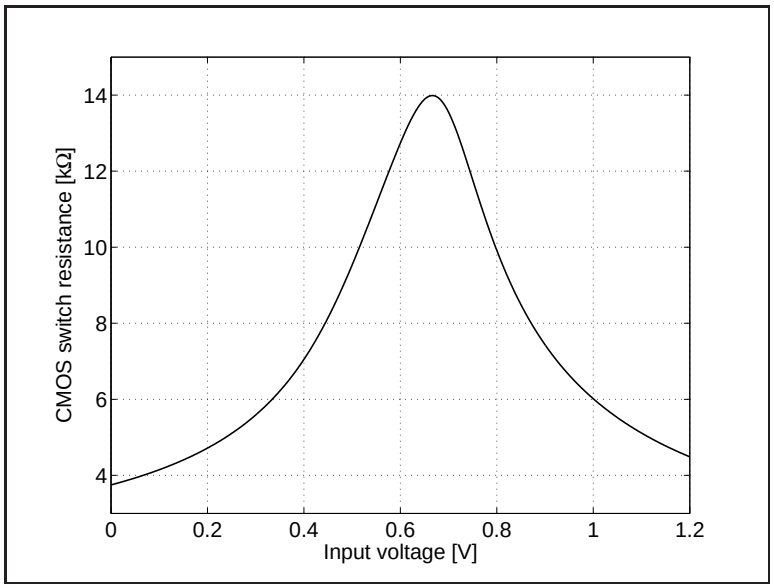


FIGURE 3.5. Variation of the CMOS switch resistance versus the input voltage.

3.2.1.3. Layout Considerations in a Two-rail DAC Architecture

In a two-rail DAC architecture, the main nodes V_{cp} and V_{cm} must be carefully implemented. On the first step of the conversion, capacitors C_1 and C_2 are connected to these nodes to begin the passive charge-sharing process. If the nodes V_{cp} and V_{cm} have a large capacitance connected to ground or a large capacitance between them compared to the unity capacitance, then a considerable voltage attenuation occurs in the final capacitor nodes. This problem is equivalent to adding a third capacitor connected in the charge-sharing process, but with an initial voltage equal to zero. Although this effect is mitigated in the following conversion steps, the performance is still affected.

In order to reduce the parasitic capacitance connected to nodes V_{cp} and V_{cm}, the separation between the DAC standard cells must be large enough to ensure no missing codes, causing a larger die size area in comparison with a cascade DAC architecture.

3.3. Dynamic Comparator

The dynamic comparator implemented is shown in Figure 3.6. It consists of a differential pair and a cross-coupled inverter (Hajimiri & Heald, 1998). This topology is often used in low-power SAR ADCs (Craninckx & Van der Plas, 2007), (Van Elzakker et al., 2008), (Nuzzo et al., 2009). Table 3.2 indicates the transistor sizes used in the final implementation. PMOS transistor are used as inputs, because according to the process statistical coefficients, they have lower threshold voltage variation (IBM, 2010).

TABLE 3.2. Dynamic comparator transistor sizes. For all transistors, $L = 0.12$ μm.

Transistor	Width [μm]	Transistor	Width [μm]	Transistor	Width [μm]
M_1	0.32	M_6	0.64	M_{11}	0.16
M_2	5.12	M_7	0.64	M_{12}	0.32
M_3	5.12	M_8	0.16	M_{13}	0.32
M_4	1.28	M_9	0.16	M_{14}	0.16
M_5	1.28	M_{10}	0.16	M_{15}	0.16

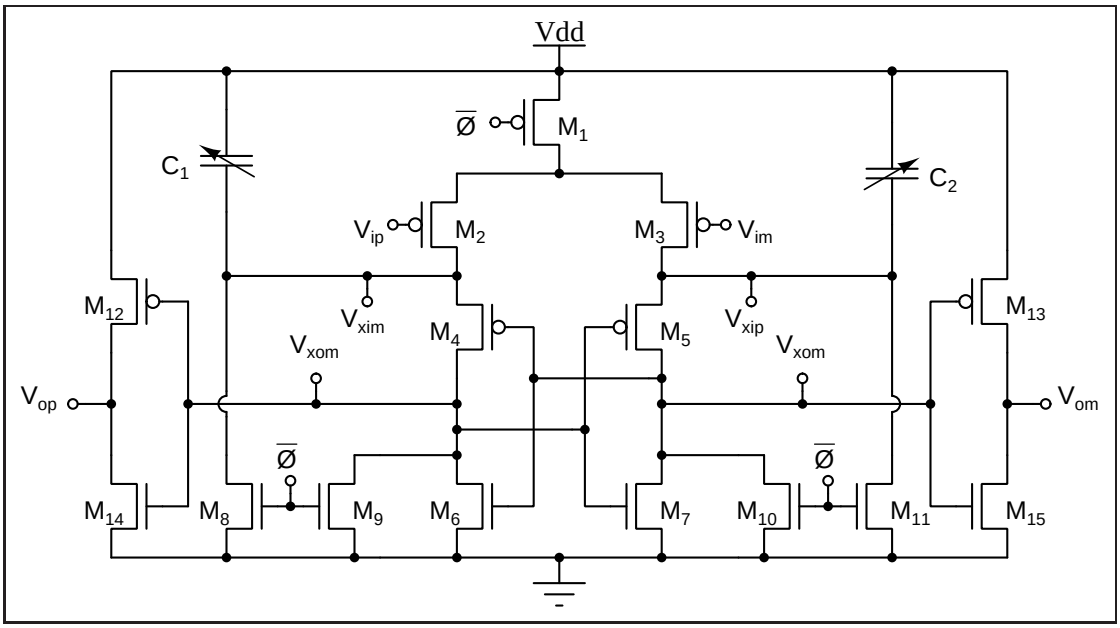


FIGURE 3.6. Dynamic comparator schematic.

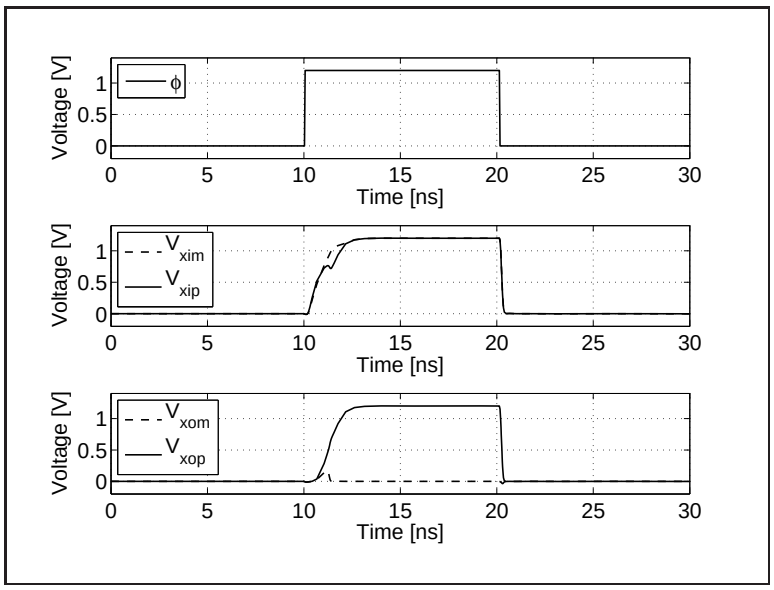


FIGURE 3.7. Dynamic comparator waveform example for an input voltage of 10 mV.

3.3.1. Circuit Operation

The operation of the circuit is as follows: when the $\overline{\phi}$ is low, transistor M_1 supplies current to the differential pair constituted by M_2 and M_3. The differential pair causes a difference of the current on each inverter pair, $M_{4,6}$ and $M_{5,7}$. The difference of current on each branch will cause that nodes V_{xim} and V_{xip}, initially at zero, increase. However, there will be a small difference on these voltages depending on the differential input voltage. This difference will drive one of the inverter to change its state before the other, and also forcing to trigger the cross-coupled inverter in the opposite direction, resulting a positive feedback. Through this, each of the two outputs of the comparator, V_{xop} and V_{xom}, reach an opposite rail voltage depending on the sign of the differential input voltage. The procedure explained above is diagrammed in Figure 3.7.

Transistors $M_{8,9,10,11}$ are NMOS switches to reset the V_{xim}, V_{xip}, V_{xom} and V_{xop} and ensure that all the transistors reset their state before a new step conversion is begin. The output inverters formed by the pairs $M_{12,14}$ and $M_{13,15}$ buffer the output of the comparator to the rest of the circuit, thus a difference in the capacitive load outside the comparator block does not degrade the performance. Finally C_1 and C_2 are variable capacitors to calibrate the comparator input offset.

3.3.2. Circuit Design

In this section, the comparator design is explained in order to maximize the performance of the PRS SAR ADC.

3.3.2.1. Speed and Input Voltage Offset

To reduce the input-referred offset voltage, the bias current of the comparator must be set to its minimum (Wicht, Nirschl, & Schmitt-Landsiedel, 2004). However, reducing the bias current reduces the speed of the comparator, which implies larger delays when the differential input voltage is small. Therefore, there is a tradeoff between the speed and the input offset of the comparator.

As the speed in the PRS SAR ADC is already limited by the RC network of the DAC array, it is preferable to reduce the offset voltage than increasing the speed. To reduce the tail current, transistor M_1 size is set to the minimum. Also, reducing the input voltage common mode helps to reduce the tail current, but this value is set to $V_{ref}/2$ to increase the input voltage range of the ADC.

3.3.2.2. Input-referred Noise

The dynamic behavior of the latched comparator makes the noise analysis difficult. However, in (Nuzzo et al., 2008) an approach to reduce the input referred noise on dynamic comparators is presented. In order to reduce the noise, the width transistors ratios $W_{2,3}/W_1$ and $W_{4,5}/W_1$ must be large. Where the ratio $W_{2,3}/W_1$ have a greater impact in the noise reduction, than ratio $W_{4,5}/W_1$

Also, increasing the width $W_{2,3}$ helps to reduce of the input-referred offset voltage, because the threshold voltage variation coefficient decreases (Pelgrom, Duinmaijer, & Welbers, 1989). Thus, the ratios are set as $W_{2,3}/W_1 = 16$ and $W_{4,5}/W_1 = 4$.

3.3.2.3. Offset Calibration

To reduce the input voltage offset, a calibration circuit is needed. By a MC simulation in Eldo (Mentor Graphics), the input-referred offset can be obtained for the final implementation. Figure 3.8 shows the results.

The calibration method used is the proposed in (Lee, Dally, & Chiang, 2000). The operation principle is based on changing the capacitance of the load in the V_{xim} and V_{xip} nodes to unbalance the differential current and counteract the input offset. The variable capacitor is made by an array of binary sized NMOS transistors. On each transistor the drain and source terminal are connected to the comparator nodes V_{xim} and V_{xip}, while the gate is connected to an external pad. If the gate is high, the NMOS operates in the triode zone incrementing the capacitance to supply voltage. On the other hand, is the gate is low, the NMOS operated as a dummy transistor connected to ground, adding only an overlap capacitance. Figure 3.9 describes a 3-bit example.

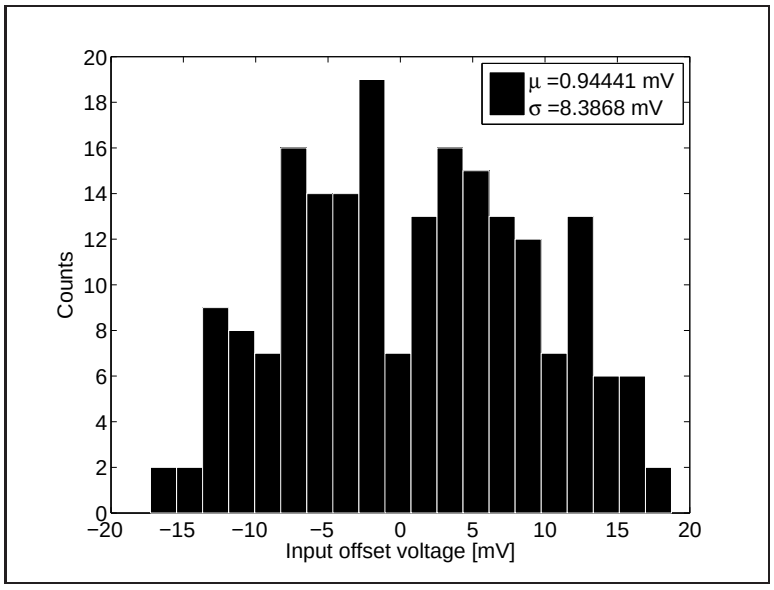


FIGURE 3.8. Histogram of the input-referred offset voltage of the dynamic comparator.

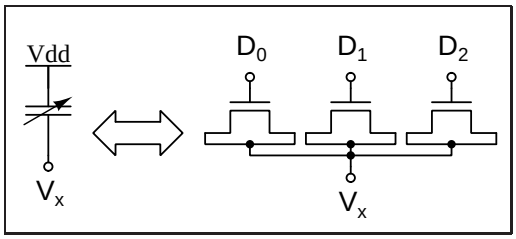


FIGURE 3.9. 3-bit variable capacitor built by NMOS transistors.

Using a 6-bit binary weighted transistor a calibration system can change the offset voltage between 0 to 20 mV with a step of 1 mV.

3.4. SAR Logic

This section explains the design and implementation of the SAR logic. In order to keep a low power consumption and reduced die area, a synthesised design flow is used.

3.4.1. Digital Logic

The function of the SAR logic is to generate all the control signals of the CMOS switches depending on the actual state (i) and the output of the comparator (cmp). These control signals are the sampling control signal (R), the successive approximation direct and cross connection control signals (sa_d and sa_c), the reference-sharing control signal (rs) and an auxiliary variable (sa_d_aux) to connect the first capacitor in the array. Also, the SAR logic must store the data output of the ADC (b). The following pseudo code explains in a simply manner the SAR logic functionality.

```
1  cmp ; \\comparator signal
2  R=1 ; \\ sampling process
3  for i, i++, i=B
4  {
5          R=0 ; \\ reset control signals
6          rs=0;
7          sa_d_aux=0;
8          if (i==1)
9                sa_d_aux = 1 ;
10         if (cmp > 0) \\succesive approximation
11              sa_d[i] = 1, sa_c[i] = 0 ;
12         else
13              sa_d[i] = 0, sa_c[i] = 1 ;
14         rs[i] = 1 ; \\reference sharing;
15         b[i] = cmp ; \\digital data
16 }
```

The pseudo code can be implemented using a finite state machine. Figure 3.10 describes the state diagram for an 8 bit implementation. Signals sa_d, sa_c, sa_d_aux and b depend on the current state and the comparator output, thus are defined as registers. On the other hand, signals R and rs only depend on the current state, thus they are defined as a result of combinational logic of the state registers.

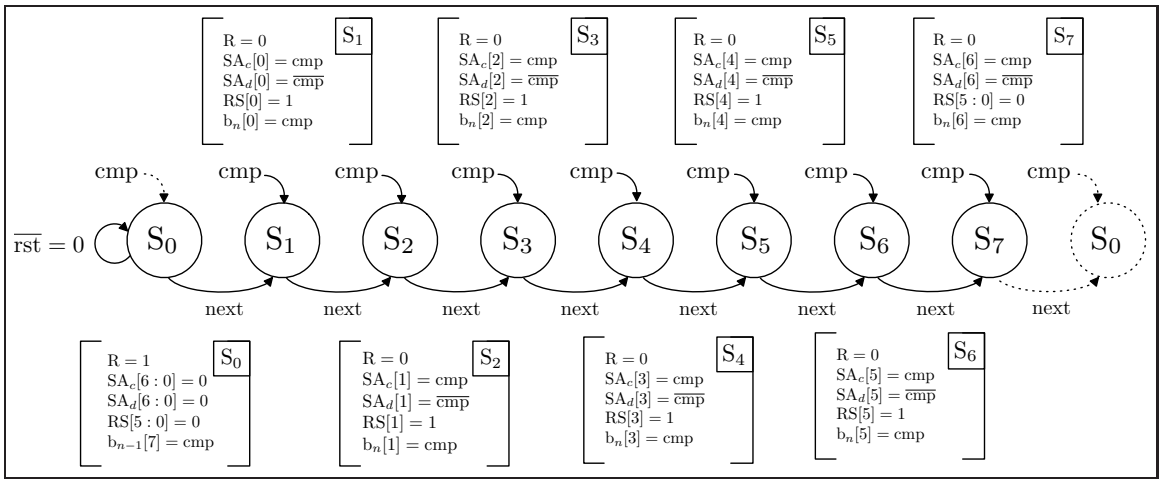


FIGURE 3.10. SAR logic finite state machine for a 8-bit implementation.

3.4.2. Timing Diagram

To avoid timing issues, the SAR logic operation is divided in to two non-overlapping cycles. The first cycle is to store the comparator output and to change the current state. The second cycle resolves the combinational logic for the control signals. In this manner, the output of comparator is always settled before its value is used to obtain the control signal, therefore no glitch or race conditions will occur. The timing diagram of digital logic is shown in Figure 3.11. The first cycle ϕ_1 starts with the positive edge of the async signal, whereas the second cycle ϕ_2 starts with the negative edge of the clock signal. The async and clock signals never overlap.

The async signal is generated with the output of the comparator and a XOR gate. When the comparator is off, clock signal high, the outputs have the same logic value, thus the async signal is low. Then, when the comparator turns on, clock signal low, the outputs diverge to opposite levels making the async signal high. Since the async input depends on a final state of the comparator, the value stored by the output comparator register is always a valid value. Using this asynchronous scheme, there is no need to use two-cycle clock generators, reducing significantly the digital power consumption.

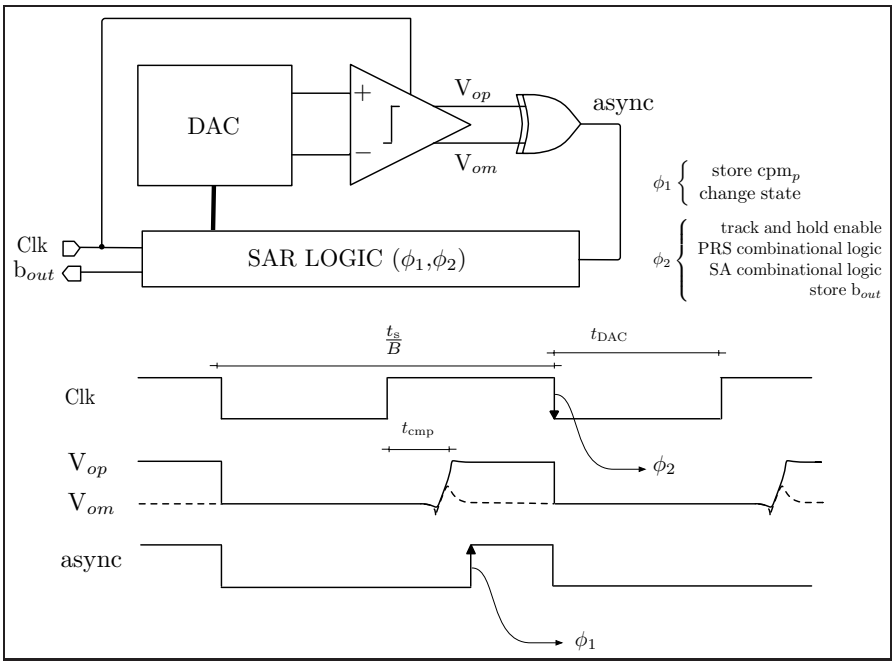


FIGURE 3.11. Digital logic timing diagram.

3.4.3. Digital Flow and Layout Implementation

The entire digital logic is implemented in a Verilog HDL environment, the complete code is included in Appendix C. This module was synthesized using Synopsys Design Compiler, resulting in a digital circuit constructed with ARM digital cells. Finally, the place-and-route of the design is made using Synopsys IC Compiler, obtaining a GDSII file.

3.5. Layout implementation

The final solid-state implementation for a PRS SAR ADC is shown in Figure 3.12 with an area of 0.024 mm^2. The complete chip implementation is included in the Appendix D and contains two PRS SAR ADCs and two dynamic comparators.

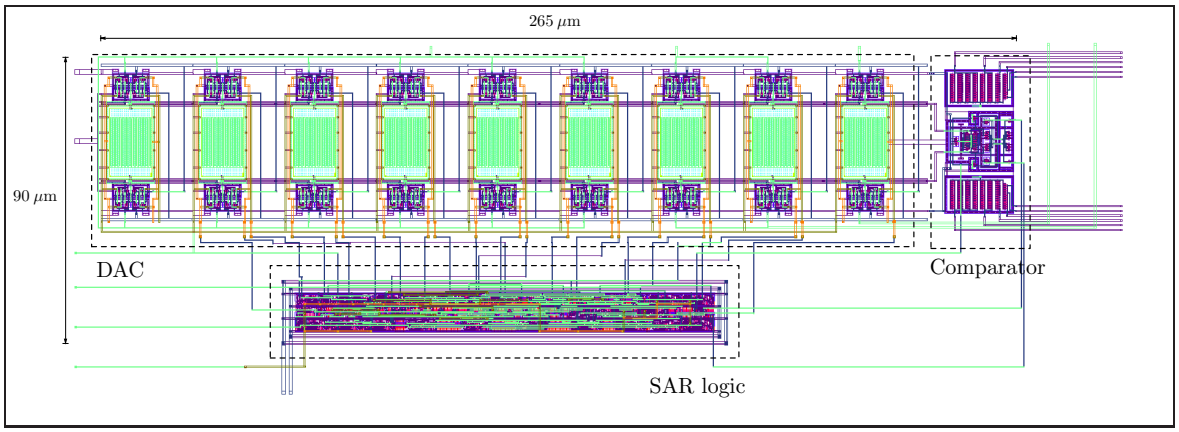


FIGURE 3.12. Layout implementation of the PRS SAR ADC.

4. POSTLAYOUT SIMULATION AND RESULTS

In this chapter the test and operation results of the ADC are presented. It is important to remark that these results are obtained with post-extraction simulations to corroborate an optimized design, thus is not the actual performance of a solid-state integrated circuit. Also, to avoid convergence problems and excessive simulation time, some simplifications on the ADC have been made, such as not considering the pads and density fill cells, and considering a offset calibrated comparator.

First the simulations tests are explained. Then, the power calculation for each individual block is presented. Finally, the results of the simulations are shown and a characterization of the ADC is obtained using the Walden figure of merit.

4.1. Test Setup

The following tests are done in order to obtain the performance of the ADC. This method is well documented in the literature (Kester & Analog Devices, 2005) and is oriented for a laboratory test.

4.1.1. Static Tests

The static tests is used to obtain static performance parameters, such as non linearities (DNL and INL). Among the most popular static tests are those based on histograms. This involves to collect a large number of digital outputs for an input analog with a well-known probability density. As the input signal statistics are known, the ADC non-linearities can be obtained by studying the resulting histogram.

Usually an input sine wave is used, because is easier to obtain in a laboratory with lower noise and distortion than other waves. However, as the result are obtained by simulations, there are no restrictions with respect to the input signal waveform. A linear ramp input is used, because the probability density of a ramp is a uniform distribution. The histogram will reveal the number of occurrences h on each k-th bin, what can be also understood as related to the width of each bin. Therefore, assuming an ideal width as the

average value[3] of the histogram $\overline{h}$, using the definition in (1.1), the DNL is obtained as

$$\mathrm{DNL}(k) = \frac{h(k) - \overline{h}}{\overline{h}}. \tag{4.1}$$

Calculating the INL is straightforward using the cumulative sum of the DNL.

4.1.2. Dynamic Tests

The dynamic tests are used to obtain the ac characteristics of the ADC such as the SNDR and ENOB. The traditional method is to convert many cycles of a sine wave signal and then compute the fast Fourier transformation (FFT) to obtain the frequency spectrum, from which the SNDR is measured and the ENOB is computed. Ideally an integer number of cycles is used. In a real setup, this characteristic is usually not fulfilled and window function have to be used to mitigate the non integer number of cycles, however as the results are obtained by simulations, there is no restriction respect the number of cycles.

Another consideration is to employ a prime number of cycles. If the number of cycles is an exact divisor of the sampling frequency, then the same values are going to be sampled each cycle. Therefore, the quantization error becomes deterministic and the frequency response will not be useful.

4.2. Results and Preliminary Comparisons

In this section the results of the post-layout simulation are presented. Also, preliminary comparisons with the first version of the PRS SAR ADC and other low-power ADCs are shown. These results are obtained using EDA tools, thus are not defining the real performance of the proposed ADC, however, they reveals a upper performance bound of an optimized design.

[3]The average value is obtained without considering the tails values, because the ramp has overflow hits and this will alter the sample mean.

4.2.1. Power Breakdown

The power consumption of each individual block of the PRS SAR ADC is shown in Table 4.1.

TABLE 4.1. Simulated PRS power breakdown with $V_{dd} = 1.2$ V for analog block and $V_{dd} = 1.2$ V for digital block.

Cell	Power consumption [μW]	Percentage
Capacitive DAC array	2.28	19%
Dynamic comparator	0.17	1%
SAR logic	9.33	79%
Full ADC	**11.78**	100%

The result of the power breakdown shows that the digital logic has the largest contribution to the power dissipation with approximately 79% of the total consumption. Even though in this work an optimized design of the DAC and comparator have been tailored to minimize the power consumption, the digital block sets an important limitation. For CMOS dynamic digital circuits, according to (Chandrakasan, Sheng, & Brodersen, 1992), the power dissipation is determined by

$$P_{digital} = p_t(C_L V_{dd}^2 f_{clk}) + I_{leakage} V_{dd} \tag{4.2}$$

where, p_t is an activity factor, C_L is the total capacitance in the logic gates, f_{clk} is the clock frequency and $I_{leakage}$ is the total leakage current. With the technology scaling, the gate capacitance becomes smaller, as well as the supply voltage. From this, the power consumption drawn by the digital logic of the PRS can be significantly reduced using recent technology nodes. Therefore the energy performance of the PRS SAR ADC can still improve with the technology scaling. Also reducing the supply voltage of the digital blocks can improve the power consumption, but the cell provider does not recommend to use lower voltage than 1.08 V in order to comply with the cell specifications.

On the other hand, the PRS topology allows to use smaller supply voltage value. The only limitation is to maintain noise values according to the design parameters. However, if the supply voltage is reduced to 1 V, the required minimum capacitor value for an 8-bit implementation is still below 100-fF, thus the proposed design can operate at lower supply voltages.

Although the design can be tested with smaller supply voltages, the clock period must be reduced too, causing extremely higher simulation time. For this reason, these tests will be done in a laboratory setup when the actual integrated circuit arrives from the factory.

4.2.2. Simulation Results

4.2.2.1. Static Test Results

The result of a static transfer function for an input linear ramp is shown in Figure 4.3. The DNL and INL are shown in Figures 4.1 and 4.2 and respectively.

The simulated ramp response shows a reduction in the input range, this results in a slightly reduction of the SNR. In addition, as the maximum and minimum values for the DNL are -0.91/0.93 LSB, there are no missing codes. From the DNL the critical codes are recognized, which correspond to the most significant bit transitions, such as codes 32, 64 and 96.

4.2.2.2. Dynamic Test Results

The FFT plot of the sine wave response is shown in Figure 4.4. The result of the dynamic test reveals an ENOB of 7.3 bits. The spurious tones are caused by the parasitic capacitance which, neglecting the comparator offset, are the components with higher impact on the converter linearity.

4.2.3. Characterization of the ADC

The characteristics of the proposed design for the PRS SAR ADC are summarized in Table 4.2 after simulation of the static and dynamic tests. In Figure 4.5 the proposed and the

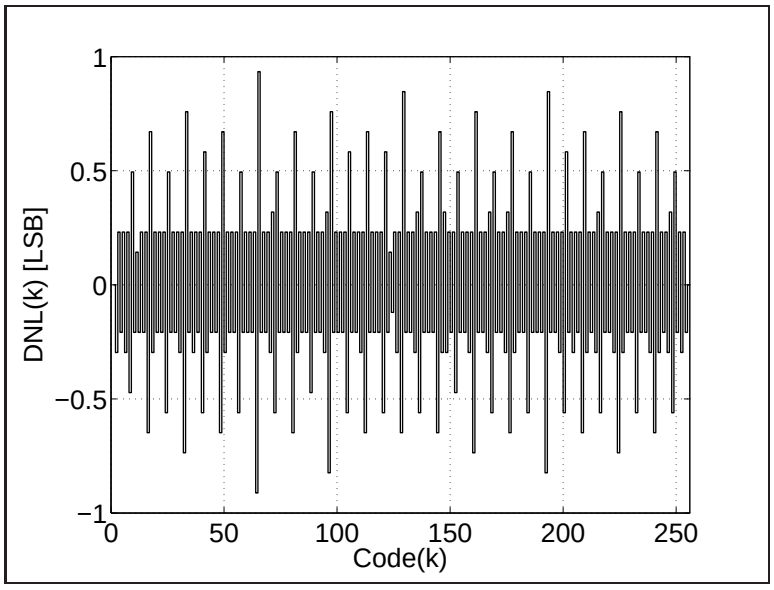


FIGURE 4.1. Simulated differential non-linearity for 3000 points and 2.08 MS/s.

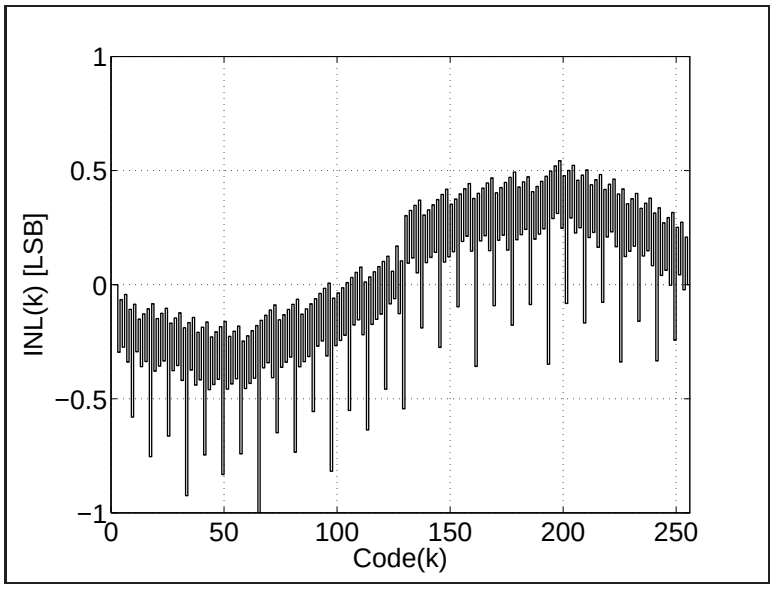


FIGURE 4.2. Simulated integral non-linearity for 3000 points and 2.08 MS/s.

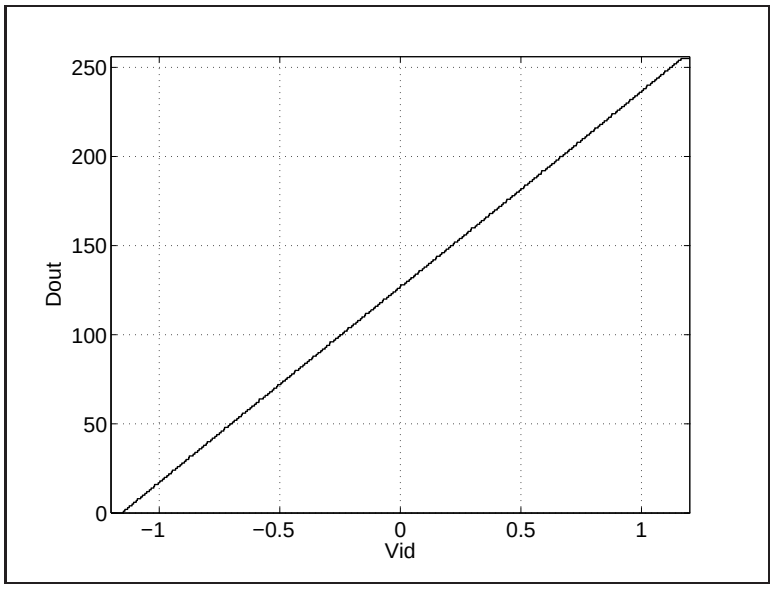


FIGURE 4.3. Static ramp response for 3000 points and 2.08 MS/s.

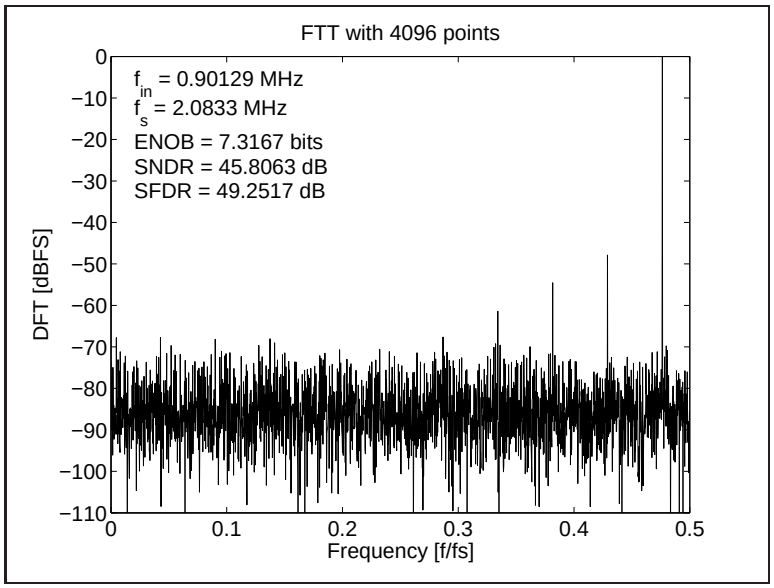


FIGURE 4.4. Output spectrum of the PRS SAR ADC for an input sine wave.

first version of the PRS SAR ADC are included in the Murmann ADC survey (Murmann, 2015) to compare the energy performance with other high-performance converters.

Compared with the first implementation of the PRS by (Alvarez-Fontecilla & Abusleme, 2015), the proposed design has a similar figure of merit and a higher resolution. Also a higher speed can be reached. At 1.5 MS/s, the proposed PRS has a power consumption of 5.7 μW, which is close to twice the power consumption of the first implementation at the same sampling rate. As the capacitor values of the DAC array are similar, the mayor difference is in the digital logic block.

Regarding the digital block, the first implementation was done in a 180 nm technology with a supply voltage of 1.2 V, whereas the proposed design is for a 130 nm technology with a supply voltage of 1.2 V. Even thought both implementations use similar supply voltage, the new design has the advantage of have smaller capacitances. On the other hand, in the proposed design the power consumption includes the asynchronous clock generation and the clock internal buffers, which are not considered in the power measurement of the first implementation (close to 29 μW). Therefore, to make a fair comparison, the test result from both designs must reported for the same conditions.

4.2.4. Data Converter for Biomedical Applications

With a small die area and high energy efficiency, the proposed design of the PRS SAR ADC is suitable for ultra low power applications, such as biomedical circuits. Compared with recent work in low power converters, this design has competitive levels in terms of power dissipation and speed, being the small die area the most important feature of this design. Table 4.3 summarized this comparison with other recent works in low-power data converters and medium resolution: (Jeong et al., 2015; Zhang et al., 2012; Harpe et al., 2011; Tsai, Chen, Shen, & Huang, 2011).

TABLE 4.2. Results of the proposed design of the PRS SAR ADC.

Number of bits (B)	8 bits
Technology process	0.13 μm
Die area	0.024 mm^2
Total capacitance	900 fF
Clock frequency	16.67 MHz
Sampling frequency (f_s)	2.08 MS/s
Total power	11.78 μW
DNL@f_s	-0.91/0.93 LSB
INL@f_s	-1.09/0.54 LSB
SNDR@f_s	45.81 dB
ENOB@f_s	7.32 bits
FOM	35.4 fJ/conv-step

TABLE 4.3. Comparison with recently work in low-power ADC.

	This work	Joeng 2015	Zang 2012	Harpe 2011	Tsai 2011
Resolution [bit]	**8**	8	10	8	8
Technology [nm]	**130**	130	130	90	90
Die area [mm^2]	**0.024**	0.120	0.190	0.055	0.056
Sampling freq. [MS/s]	**2.083**	0.10	0.001	10.24	40
Total power [μW]	**11.78**	0.12	0.072	26.3	127
ENOB [bit]	**7.32**	7.5	9.1	7.8	7.75
FoM [fJ/conv-step]	**35.4**	6.6	94.5	12	20

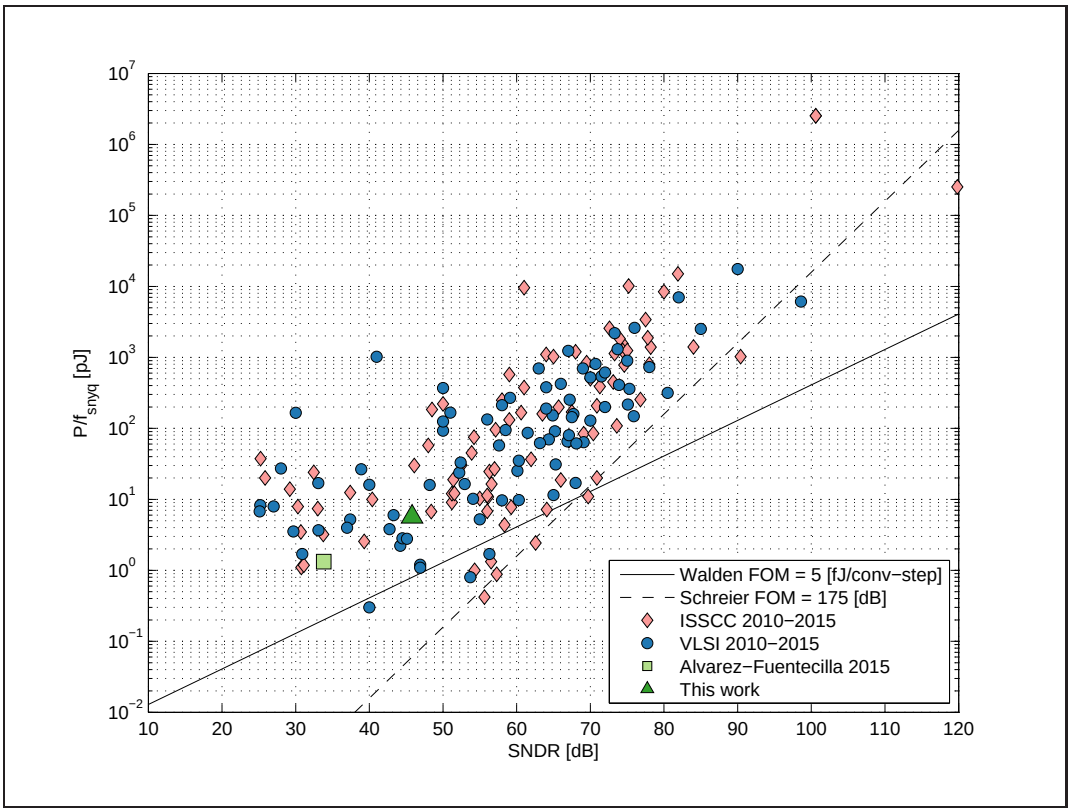


FIGURE 4.5. Comparison in terms of energy of the proposed design for the PRS SAR ADC.

5. CONCLUSION

A complete review of the passive reference-sharing topology has been made in order to explore and optimize its operation limits. Based on this analysis, a fully differential 8-bit, $2.08\ M$S/s, $11.78\ \mu$W and 7.3 ENOB ADC is proposed and implemented using a 130 nm technology process, using a die area of 0.024 mm^2. Compared with the original design, the major improvements are an enhancement in the resolution and speed. Also, a FOM of $35.4\ f$J/conv-step is obtained in a preliminary simulation, which reveals a similar figure of merit as the first version. Among the features of the new design, there are a faster DAC array architecture, a complete digital synthesis for the SAR logic, and an asynchronous clock to trigger the logic avoiding the use of two-phased non-overlapping clock.

According to the power breakdown analysis, the digital logic is the larger contributor to the power consumption. With the technology scaling, digital circuits have an important energy reduction, because of smaller capacitance and supply voltage. Therefore, as the power consumption is still limited by the digital block, a significant reduction can be obtained by implementing this design in smaller technology node or using a lower supply voltage.

Regarding the state of the art, the proposed ADC presents a 50% reduction in the die area compared with the smallest work reported for a 8-bit resolution converter, being the most attractive feature. In addition, the resulting Walden FOM is in the same order of magnitude of the other works reported. To achieve an efficiency similar closer to performance limits reported in Figure 4.5 (5 fJ/conv-step), the proposed design must reduce its energy per conversion in 86%. The low-power operation, medium resolution and extremely small die area, makes the PRS ADC a suitable converter for low-power wireless devices, specially for biomedical sensing SoC and WSN modules. This characteristics makes the passive reference-sharing architecture an important contribution in the low-power ADC research area.

Finally, a successfully mixed-signal design flow is implemented for a 130 nm process. With this design flow, a full chip has been taped out within the MOSIS academic research

program. This contribution will allow to implement mixed-signal integrated circuits in a more advanced technology node.

5.1. Future Work

In the short term, the proposed design of the PRS SAR ADC must be tested after fabrication. The test result of the solid-state implementation will allow to test the improvements of the new design. The test-bench of the ADC includes the design of a printed circuit board (PCB) to include the chip, power supply and DACs to provide the stimuli in the analog domain. Also a field programmable gate array (FPGA) will be used to generate the input signals in the digital domain, the clock and the reset signals, and to store the digital output. Then, the output data can be processed by computing calculation and obtaining the performance metric.

In the long term, two improvements of the ADC implementation can be done. First to achieve faster speed, time-interleaving techniques can be used. Second, using more recent technologies and lower supply voltage, the power consumption of the digital block can be reduced to be comparable with the power consumption of the analog block. With this two enhancement, the PRS converter will be approaching to their performance limits.

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APPENDIX

APPENDIX A. EQUIVALENCE IN PASSIVE CHARGE SHARING

To facilitate the analysis of the passive charge-sharing process, an equivalence between serial and parallel connections is proposed. In Figure A.1 the circuit equivalence are shown where r, l and m subscripts correspond to right, left and middle, respectively. To prove the equivalence both of the two serial and parallel charge-sharing processes are resolved individually and then their results are compared.

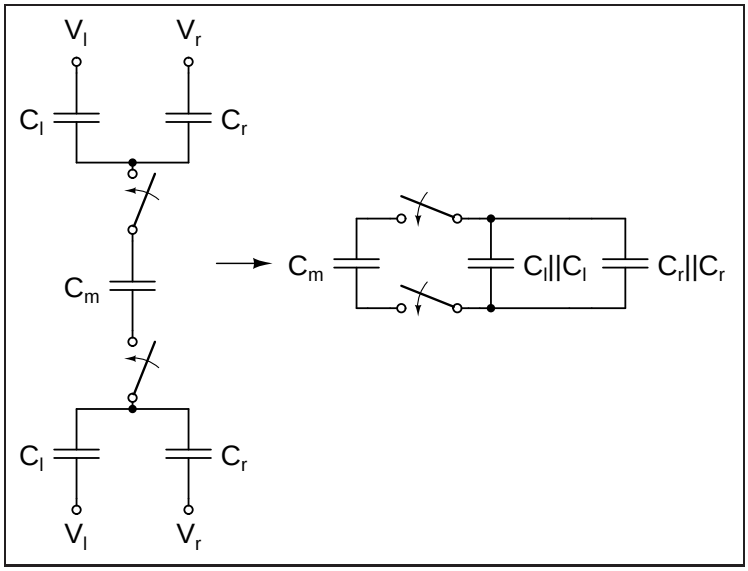

FIGURE A.1. Passive sharing process equivalence.

A.1. Series Passive Charge-Sharing

In Figure A.2 the series passive charge-sharing process is shown. The initial charge in the nodes V_t y V_b are

$$Q_{t,i} = (V_t' - V_r)C_r + (V_t' - V_l)C_l + C_m V_m' \tag{A.1}$$

$$Q_{b,i} = (-V_b' + V_r)C_r + (-V_b' + V_l)C_l + C_m V_m' \tag{A.2}$$

The charge at the end of the process in the nodes V_t y V_b are

$$Q_{t,f} = (V_t - V_r)C_r + (V_t - V_l)C_l + C_m V_m \tag{A.3}$$

$$Q_{b,f} = (-V_b + V_r)C_r + (-V_b + V_l)C_l + C_m V_m \tag{A.4}$$

As the nodes V_t y V_b do not have any external connection, the charge must be equal on each stage of the sharing process. Therefore, the initial charge is equal to the final charge, then solving for $V_t - V_b$, the final voltage in the C_m capacitor is written as

$$V_t - V_b = V_m = \frac{(V_t' - V_b')(C_r + C_l) + 2C_m V_m'}{C_r + C_l + 2C_m}. \tag{A.5}$$

Equation (A.5) reveals that the voltage in the C_m capacitor does not depend on the V_r and V_l voltages. From this, it can be assumed that those voltages are connected to ground to facilitate the algebra.

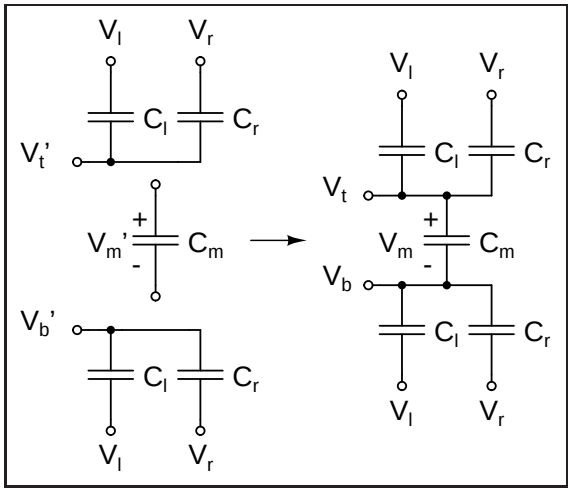

FIGURE A.2. Series passive charge-sharing process.

A.2. Parallel Passive Charge-Sharing Process.

In Figure A.3 the series passive charge sharing process is shown. The initial charge in the nodes V_t y V_b are

$$Q_{tb,i} = (V_t' - V_b') \left(\frac{C_r}{2} + \frac{C_l}{2} \right) + C_m V_m' \tag{A.6}$$

The charge at the end of the process in the nodes V_t and V_b are:

$$Q_{tb,f} = (V_t - V_b) \left(\frac{C_r}{2} + \frac{C_l}{2} \right) + C_m V_m \tag{A.7}$$

Equating the above charge expression and solving for $V_t - V_b$, the final voltage in the C_m capacitor is written as

$$V_t - V_b = V_m = \frac{(V_t' - V_b')(C_r + C_l) + 2C_m V_m'}{C_r + C_l + 2C_m}. \tag{A.8}$$

Expressions (A.5) and (A.8) are equal, therefore the equivalence is correct.

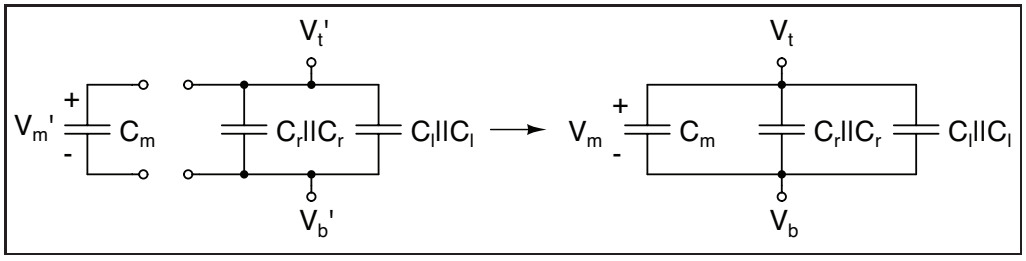

FIGURE A.3. Parallel passive charge-sharing process.

APPENDIX B. NOISE FACTOR $f(B)$ 4-BIT EXAMPLE

The noise contribution in the passive reference-sharing process and in the sampling process is determined by equation (2.24). As the computation of the noise factor $f(B)$ is not obtained by a closed-form expression, a 4-bit example is explained based on the work by (Alvarez-Fontecilla & Abusleme, 2015). This analysis can be extended to any higher resolution.

In a generic sampling circuit, every time a switch is opened, a kT/C noise contribution is added in the hold capacitor (Pelgrom, 2010). Therefore, in the DAC array, after the sampling process is finished, each capacitor will hold a voltage noise power of kT/C. Then, after the reference sharing-process is finished, as the involved capacitors share their initial charges, they will also share a fraction of its initial voltage noise power. In addition, a KT/C noise contribution is again added due to the switch aperture.

Let us define kT/C_i the noise power at the capacitor C_i after the track-and-hold process, $kT/C_{i,i-1}$ the noise contribution added to capacitors C_i and C_{i-1} after the reference-sharing process, and $\overline{v_{nC_i}^2}$ the total integrated noise at each capacitor.

As a 4-bit conversion required only one sampling process and two reference-sharing process, the obtention of the voltage noise power is explained in three steps. The subscript of this example is consistent with Figure 1.13.

First, after the track-and-hold process, each capacitor hold a kT/C voltage noise power, then the voltage noise power on each capacitors is given by

$$\overline{v_{nC_0}^2} = \left(\frac{kT}{C}\right)_0 \tag{B.1}$$

$$\overline{v_{nC_1}^2} = \left(\frac{kT}{C}\right)_1 \tag{B.2}$$

$$\overline{v_{nC_2}^2} = \left(\frac{kT}{C}\right)_2 \tag{B.3}$$

$$\overline{v_{nC_3}^2} = \left(\frac{kT}{C}\right)_3 \tag{B.4}$$

$$\overline{v_{n_{C_4}}^2} = \left(\frac{kT}{C}\right)_4 . \tag{B.5}$$

Second, during the first passive reference-sharing process, capacitor C_2 and C_3 will share their charge, so the initial voltage noise power will be shared in equal parts. It is important to note that the voltage noise power is shared as a signal voltage, not as a power unit. At the end of the passive-reference process, the aperture of the switches will add again a kT/C noise contribution at capacitors C_2 and C_3. Then, the voltage noise power on each capacitors is given by

$$N_{C_0} = \left(\frac{kT}{C}\right)_0 \tag{B.6}$$

$$N_{C_1} = \left(\frac{kT}{C}\right)_1 \tag{B.7}$$

$$N_{C_2} = \frac{1}{4}\left(\frac{kT}{C}\right)_2 + \frac{1}{4}\left(\frac{kT}{C}\right)_3 + \left(\frac{kT}{C}\right)_{2,3} \tag{B.8}$$

$$N_{C_3} = \frac{1}{4}\left(\frac{kT}{C}\right)_2 + \frac{1}{4}\left(\frac{kT}{C}\right)_3 + \left(\frac{kT}{C}\right)_{2,3} \tag{B.9}$$

$$N_{C_4} = \left(\frac{kT}{C}\right)_4 . \tag{B.10}$$

Third, during the second passive reference-sharing process, the same procedure is repeated for capacitor C_3 and C_4, then the voltage noise power on each capacitors is given by

$$N_{C_0} = \left(\frac{kT}{C}\right)_0 \tag{B.11}$$

$$N_{C_1} = \left(\frac{kT}{C}\right)_1 \tag{B.12}$$

$$N_{C_2} = \frac{1}{4}\left(\frac{kT}{C}\right)_2 + \frac{1}{4}\left(\frac{kT}{C}\right)_3 + \left(\frac{kT}{C}\right)_{2,3} \tag{B.13}$$

$$N_{C_3} = \frac{1}{16}\left(\frac{kT}{C}\right)_2 + \frac{1}{16}\left(\frac{kT}{C}\right)_3 + \frac{1}{4}\left(\frac{kT}{C}\right)_{2,3} + \frac{1}{4}\left(\frac{kT}{C}\right)_4 + \left(\frac{kT}{C}\right)_{3,4} \tag{B.14}$$

$$N_{C_4} = \frac{1}{16}\left(\frac{kT}{C}\right)_2 + \frac{1}{16}\left(\frac{kT}{C}\right)_3 + \frac{1}{4}\left(\frac{kT}{C}\right)_{2,3} + \frac{1}{4}\left(\frac{kT}{C}\right)_4 + \left(\frac{kT}{C}\right)_{3,4}. \tag{B.15}$$

Finally, as only the noise contribution of capacitors C_0, C_1, C_2 and C_3 are referred to the comparator input during the successive approximation process, only these power noise sources must be added. Considering that contributions with the same subscript are fully correlated and must be added as signals, the total voltage noise power of the passive reference-sharing and sampling process is given by

$$\overline{v_{n1}^2} = \sum_{i=0}^{4-1} \overline{v_{nC_i}^2} = 6.625\frac{KT}{C}. \tag{B.16}$$

APPENDIX C. SAR LOGIC VERILOG HDL CODE

C.1. PRS Logic Module

```
1  module PRS_logic (clk, clk_async, clk_n, cmp_p,
2                    rst_n, adc_out, sw_d, sw_c, sw_cmp, w_rs,r);
3
4  // Parameters
5
6  //finite state machine states, one for each bit conversion
7  parameter   [2:0]   S0 = 3'b000;
8  parameter   [2:0]   S1 = 3'b001;
9  parameter   [2:0]   S2 = 3'b010;
10 parameter   [2:0]   S3 = 3'b011;
11 parameter   [2:0]   S4 = 3'b100;
12 parameter   [2:0]   S5 = 3'b101;
13 parameter   [2:0]   S6 = 3'b110;
14 parameter   [2:0]   S7 = 3'b111;
15
16 // Input Ports
17
18 input               clk; //master clock
19 input               clk_n; //master clock complement
20 input               clk_async; //asynchronous clock
21 input               rst_n; //negative active reset
22 input               cmp_p; //comparator output
23
24 // Output Ports
25 output reg          adc_out; //adc output on each conversion cycle
26 output reg  [6:0]   sw_d; //direct switch control signal for SA process
27 output reg  [6:0]   sw_c; //cross switch control signal for SA process
28 output reg          sw_cmp; // switch control signal for 1st conversion
29 output      [5:0]   sw_rs; //switch control signal for RS process
30 output              r; //track and hold control signal
```

```
31
32 // Auxiliar Variables
33 reg         [2:0]   state; //present state
34 reg                 cmp_aux; //to store cmp_p signal
35 wire        [6:0]   one_shot; //one shot state variable
36 wire        [2:0]   next; //next stage
37
38 // Modules
39 bin2oneshot inst_1  (.x(state),.y(one_shot)); //one shot states
40 state2next  inst_2  (.x(state),.y(next)); //logic to get next state
41
42 // Phi_1
43 //trigger by the asynchronous signal
44 always @ ( posedge clk_async or negedge rst_n )
45   begin
46     if ( !rst_n ) //state 0 until the rst_n is high
47       begin
48         state     <=    S0;
49         cmp_aux   <=    1'b0;
50       end
51     else //the sar logic begins
52       begin
53         state     <=    next;
54         cmp_aux   <=    cmp_p; //store the comparator output
55       end
56     end
57   end
58
59 // Phi_2
60 //trigger by the master clock
61 always @ ( negedge clk )
62   begin
63     case ( state )
64       S0 : //reset variables, track and hold, and 8th bit is obtained
```

```
65          begin
66            sw_d      =   7'd0; //reset
67            sw_c      =   7'd0; //reset
68            adc_out   =   cmp_aux; //LSB of previous conversion
69            sw_cmp    =   1'b0; //reset
70          end
71        S1 :  //1st bit is obtained
72          begin
73            sw_d[0]   =   !cmp_aux; //close switch if cmp_p = 0
74            sw_c[0]   =   cmp_aux; //close switch if cmp_p = 1
75            adc_out   =   cmp_aux; //D0 output
76            sw_cmp    =   1'b0; //connect 1st capacitor to comparator
77          end
78        S2 :  //2nd  bit is obtained
79          begin
80            sw_d[1]   =   !cmp_aux;
81            sw_c[1]   =   cmp_aux;
82            adc_out   =   cmp_aux; //D1 output
83          end
84        S3 : //3rd  bit is obtained
85          begin
86            sw_d[2]   =   !cmp_aux;
87            sw_c[2]   =   cmp_aux;
88            adc_out   =   cmp_aux; //D2 output
89          end
90        S4 : //4th  bit is obtained
91          begin
92            sw_d[3]   =   !cmp_aux;
93            sw_c[3]   =   cmp_aux;
94            adc_out   =   cmp_aux; //D3 output
95          end
96        S5 : //5th  bit is obtained
97          begin
98            sw_d[4]   =   !cmp_aux;
```

```
99            sw_c[4]   =   cmp_aux;
100           adc_out   =   cmp_aux; //D4 output
101         end
102       S6 : //6th  bit is obtained
103         begin
104           sw_d[5]   =   !cmp_aux;
105           sw_c[5]   =   cmp_aux;
106           adc_out   =   cmp_aux; //D5 output
107         end
108       S7 : //7th  bit is obtained
109         begin
110           sw_d[6]   =   !cmp_aux;
111           sw_c[6]   =   cmp_aux;
112           adc_out   =   cmp_aux; //D6 output
113         end
114     endcase
115   end
116
117 //Track and hold control signal.
118 //Its only valid when the clock is low (&clk_n) to avoid timing
119 // overlaps.
120 //If the state parameters were defines as a one-shot code, the r signal
121 // is equal to the less significant bit.
122 assign r = one_shot[0]&clk_n;
123
124 //RS control signals.
125 //Its only valid when the clock is low (&clk_n) to avoid timing
126 // overlaps.
127 //The rs signal waveform is equal to a one-shot truth table.
128 assign sw_rs [5:0] = one_shot[6:1]&{clk_n,clk_n,clk_n,clk_n,clk_n,clk_n};
129
130 endmodule
```

C.2. Auxiliary Modules

```
1  module state2next(x,y);
2  //combinational logic to pass the actual state
3  //to the last state. Equal to a 3-bit + 1'1b operation
4  //The logic is the result of solving the truth table
5
6  input   [2:0]   x;
7  output  [2:0]   y;
8
9  assign  y[0]  = !x[0];
10 assign  y[1]  =  x[1] && !x[0] || !x[1] &&  x[0];
11 assign  y[2]  =  x[2] && !x[1] ||  x[2] && !x[0] || !x[2]  &&  x[1]  &&
   x[0];
12
13 endmodule
```

```
1  module bin2oneshot(x,y);
2  //combinational logic to pass a binary code to
3  //a one-shot code.
4  //The logic is the result of solving the truth table
5
6  input       [2:0]   x;
7  output      [6:0]   y;
8
9  assign  y[6]  =  x[2] &&  x[1] && !x[0];
10 assign  y[5]  =  x[2] && !x[1] &&  x[0];
11 assign  y[4]  =  x[2] && !x[1] && !x[0];
12 assign  y[3]  = !x[2] &&  x[1] &&  x[0];
13 assign  y[2]  = !x[2] &&  x[1] && !x[0];
14 assign  y[1]  = !x[2] && !x[1] &&  x[0];
15 assign  y[0]  = !x[2] && !x[1] && !x[0];
16
17 endmodule
```

C.3. Top Module

```
1  module top(clk, clk_n, cmp_p, cmp_m, adc_out, sw_d , sw_c, sw_rs,
2    sw_cmp, r, rst_n);
3
4  // Input Ports
5  input           clk; // master clock
6  input           cmp_p; // positive comparator output
7  input           cmp_m; // negative comparator output
8  input           rst_n; // low active reset
9
10 // Output Ports
11 output          adc_out; //converter digital output
12 output  [6:0]   sw_d; //direct switch control signal for SA process
13 output  [6:0]   sw_c; //cross switch control signal for SA process
14 output  [5:0]   sw_rs; //switch control signal for RS process
15 output          sw_cmp;  // switch control signal for 1st conversion
16 output          r; //track and hold control signal
17 output          clk_n; //comparator trigger signal
18
19 // Auxiliary signals
20 wire            clk_async; //asynchronous clock
21
22 // Combinational logic
23 //asynchronous clock generation for PRS logic
24 assign  clk_async = cmp_p ^ cmp_m;
25 //master clock complement for comparator trigger signal
26 assign  clk_n     = !clk;
27
28 // Modules
29 PRS_logic inst_1 (.clk(clk), .clk_async(clk_async), .clk_n(clk_n),
30       .cmp_p(cmp_p), .rst_n(rst_n), .adc_out(adc_out), .sw_d(sw_d),
31       .sw_c(sw_c), .sw_cmp(sw_cmp), .sw_rs(sw_rs), .r(r) );
32 endmodule
```

APPENDIX D. RAIDEN PROTOTYPE PINOUT

RAIDEN prototype has 66 ports and was bonded to a 100-lead package from Kyocera Corporation. The package part number corresponds to QC-100365-WZ. The RAIDEN full chip is shown in Figure D.1. Table D.1, D.2, D.3 and D.4 show the RAIDEN pinout.

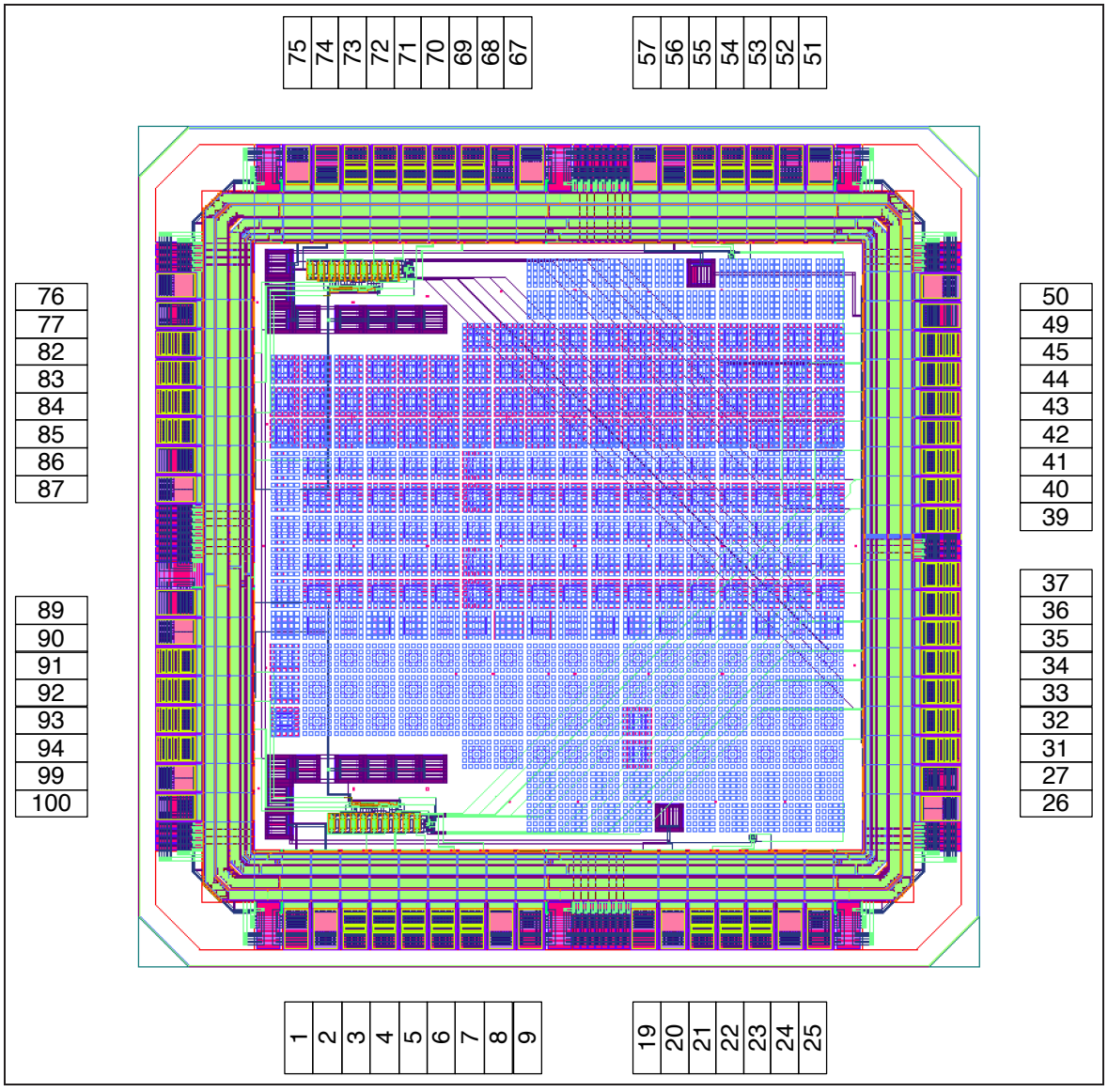

FIGURE D.1. RAIDEN chip.

TABLE D.1. RAIDEN prototype pinout 1-25

Pin number	Pin name	Description
1	AGND	Analog ground.
2	PRS_2_AVDD	Analog supply voltage for second ADC.
3	PRS_2_VCM	Common mode voltage reference for second ADC.
4	PRS_2_VRP	Positive voltage reference for second ADC.
5	PRS_2_VIP	Positive input voltage for second ADC.
6	PRS_2_VIM	Negative input voltage for second ADC.
7	PRS_2_VRM	Negative voltage reference for second ADC.
8	PRS_2_APORT_VDD	Positive supply for analog ports in second ADC.
9	PRS_2_APORT_VSS	Negative supply for analog ports in second ADC.
10	N.C.	Not connected.
11	N.C.	Not connected.
12	N.C.	Not connected.
13	N.C.	Not connected.
14	N.C.	Not connected.
15	N.C.	Not connected.
16	N.C.	Not connected.
17	N.C.	Not connected.
18	N.C.	Not connected.
19	AGND	Analog ground.
20	CMP_2_AVDD	Analog supply voltage for second comparator.
21	CMP_2_VIP	Positive input voltage for second comparator.
22	CMP_2_VIM	Negative input voltage for second comparator.
23	CMP_2_VOP	Output voltage for second comparator.
24	CMP_2_APORT_VDD	Positive supply for ports in second comparator.
25	CMP_2_APORT_VSS	Negative supply for ports in second comparator.

TABLE D.2. RAIDEN prototype pinout 26-50

Pin number	Pin name	Description
26	DIG_DPORT_VDD	Positive supply for digital ports in calibration.
27	DIG_DPORT_VSS	Negative supply for digital ports in calibration.
28	N.C.	Not connected.
29	N.C	Not connected.
30	N.C	Not connected.
31	CMP_2_CLK	Clock signal for second comparator
32	CAL_12	Right calibration bit 0
33	CAL_11	Right calibration bit 1
34	CAL_10	Right calibration bit 2
35	CAL_09	Right calibration bit 3
36	CAL_08	Right calibration bit 4
37	CAL_07	Right calibration bit 5
38	N.C.	Not connected.
39	CAL_06	Left calibration bit 0
40	CAL_05	Left calibration bit 1
41	CAL_04	Left calibration bit 2
42	CAL_03	Left calibration bit 3
43	CAL_02	Left calibration bit 4
44	CAL_01	Left calibration bit 5
45	N.C.	Not connected.
46	N.C.	Not connected.
47	N.C.	Not connected.
48	N.C.	Not connected.
49	AGND	Analog ground.
50	DIG_DVDD	Digital port suuply voltage.

TABLE D.3. RAIDEN prototype pinout 51-75

Pin number	Pin name	Description
51	CMP_1_APORT_VDD	Positive supply for ports in second comparator.
52	CMP_1_APORT_VSS	Negative supply for ports in second comparator.
53	CMP_1_VOP	Output voltage for first comparator.
54	CMP_1_VIM	Negative input voltage for first comparator.
55	CMP_1_VIP	Positive input voltage for first comparator.
56	N.C.	Not connected.
57	N.C.	Not connected.
58	N.C.	Not connected.
59	N.C.	Not connected.
60	N.C.	Not connected.
61	N.C.	Not connected.
62	N.C.	Not connected.
63	N.C.	Not connected.
64	N.C.	Not connected.
65	N.C.	Not connected.
66	N.C.	Not connected.
67	PRS_1_APORT_VDD	Positive supply for analog ports in first ADC.
68	PRS_1_APORT_VSS	Negative supply for analog ports in first ADC.
69	PRS_1_VRM	Negative voltage reference for first ADC.
70	PRS_1_VIM	Negative input voltage for first ADC.
71	PRS_1_VIP	Positive input voltage for first ADC.
72	PRS_1_VRP	Positive voltage reference for first ADC.
73	PRS_1_VCM	Common mode voltage reference for first ADC.
74	AGND	Analog ground.
75	PRS_1_AVDD	Analog supply voltage for first ADC.

TABLE D.4. RAIDEN prototype pinout 76-100

Pin number	Pin name	Description
76	PRS_1_DPORT_VDD	Positive supply for digital ports in first ADC.
77	PRS_1_DPORT_VSS	Negative supply for analog ports in first ADC.
78	N.C.	Not connected.
79	N.C.	Not connected.
80	N.C.	Not connected.
81	N.C.	Not connected.
82	PRS_1_R	Synchronise signal for first ADC.
83	PRS_1_OUT	Output data for first ADC.
84	PRS_1_RST	Reset signal for first ADC.
85	PRS_1_CLK	Clock signal for first ADC.
86	DGND	Digital ground.
87	PRS_1_DVDD	Digital supply voltage for first ADC.
88	N.C.	Not connected.
89	DGND	Digital ground.
90	PRS_2_DVDD	Digital supply voltage for second ADC.
91	PRS_2_CLK	Clock signal for second ADC.
92	PRS_2_RST	Reset signal for second ADC.
93	PRS_2_OUT	Output data for second ADC.
94	PRS_2_R	Synchronise signal for second ADC.
95	N.C.	Not connected.
96	N.C.	Not connected.
97	N.C.	Not connected.
98	N.C.	Not connected.
99	PRS_2_DPORT_VSS	Negative supply for digital ports in second ADC.
100	PRS_2_DPORT_VDD	Positive supply for digital ports in second ADC.