A FAST CAPACITIVE VOLTAGE MONITOR FOR LOW IMPEDANCE PULSE LINES

P. Choi and M. Favre*

Laboratoire de Physique des Milieux Ionisés
Ecole Polytechnique, 91128 Palaiseau Cedex, France

**Facultad de Física, Pontificia Universidad Católica de Chile*
Casilla 306, Santiago 22, Chile

INTRODUCTION

Accurate and reliable electrical measurements are critical issues in high voltage transmission lines for pulse power generators. Capacitive voltage monitoring is a well established technique which is widely used in this type of devices[1]. It is easy to install and compares favorable with other non-contact measuring techniques based on electro-optic effects[2]. The monitor can operate in the pure capacitive division, or self-integrating, mode for direct monitoring of the voltage or as a D-dot probe to measure the time rate of change of voltage. Different designs for fast voltage monitors in low impedance lines have been described in the literature[1,3,4,5]. However, additional difficulties exist in trying to improve the high frequency response of these monitors in the environment of a low impedance pulse line with water dielectric. The ultimate goal in capacitive voltage monitoring is a simple design, with good high frequence response, convenient attenuation ratio and long time constant measurement capability. Here we propose a new design for a capacitive voltage monitor which, in principle, satisfies most of the above requirements and is particularly suitable when applied to low impedance high voltage transmission lines. Above all, the design is intrinsically matched to the characteristics of the output cable and simple to implement.

In the following, the basic schemes of the capacitive monitor are first discussed in order to high-light the problems with high frequency design. The new design is then presented together with details of construction. Finally, the properties of the proposed monitor obtained from calculation and circuit simulation are demonstrated.

CAPACITIVE DIVIDERS

Figure 1 shows a simplified schematic of the equivalent electric circuit for a generic capacitive divider, mounted on the ground side of a high voltage transmission line. C_L represents the coupling capacitance to the live electrode, at potential V_L, and C_G is the coupling capacitance to ground. A series resistance R_S is placed at the junction of the two capacitance to pick up the measured signal. This introduces an additional resistive division with the load impedance of the signal cable, Z_0. For simplicity, additional

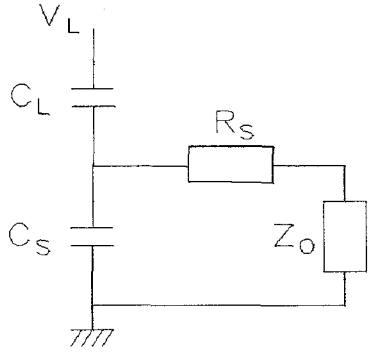

Fig.1 Equivalent circuit of a capacitive monitor

resistive elements due to finite resistivity of the dielectric media and stray inductances of the pick up resistance have not been included.

The basic circuit equation is

$$\frac{dV_L}{dt} = \frac{V_S}{RC_L} + \frac{C_L + C_G}{C_L} \cdot \frac{dV_S}{dt} \tag{1}$$

where V_S is the voltage across $R = R_S + Z_0$.

Capacitive dividers operate in two different modes depending on the characteristic time constants involved .

a) *D-dot mode*.

If

$$RC_L << \frac{C_L}{C_L + C_G} \cdot \tau \quad \text{or} \quad R(C_L + C_G) << \tau \tag{2}$$

where τ is the characteristic time of interest in the voltage signal, then

$$V_S = RC_L \cdot \frac{dV_L}{dt} \tag{3}$$

and the measured signal is proportional to the time derivative of the line voltage.

b) *Self-integrating mode.*

If

$$R(C_L + C_G) >> \tau \tag{4}$$

then,

$$V_S = \frac{C_L}{C_L + C_G} \cdot V_L \tag{5}$$

and the measured signal is directly proportional to the line voltage.

Self-integrating monitor is difficult to construct for long time constant measurements, as it can be inferred from Eq. (4). A coaxial capacitor is usually constructed for C_G in preference to discrete commercial capacitors. This minimizes the intrinsic inductance of the capacitor while providing the high working voltage rating required. The value of C_G that can be obtained this way, however, is limited in practice to the nF region and it is therefore usual to rely on a high value of R to obtain a long time constant for monitors in pulsed power measurements. This approach has the initial benefit of a further dividing ratio for very high line voltage situations, when a typical value of $Z_0 = 50\ \Omega$ is used. However, the use of a high voltage, high value resistor R_S introduces additional problems due to intrinsic and stray inductance as well as stray capacitance to ground. Both of these additional components lead to a low pass circuit and hence reduce the high frequency response of the monitor.

D-dot monitor is usually preferred when good high frequency response is required. The corresponding condition given by Eq. (2) can be easily satisfied if long time constants are involved. For shorter characteristic times the values of C_L and C_G become the crucial design parameter. The value of C_G is determined by the capacitance between the detecting tip and the body of the probe and by the stray capacitive coupling to the surrounding ground electrode. In a high voltage water pulse line environment, the separation between the live electrode and the ground electrode will be in the region of 10's of mm or more, resulting in a value of C_L of less than 1 pF for a detector tip surface area of $1 cm^2$. On the other hand, the large dielectric constant of a water surrounding provides strong coupling to the ground electrode, leading to a value of C_G at least several times that of C_L. This again introduces a low pass response into the monitor circuit.

In practice, a pure *D-dot* or pure *Self-integrating* mode is difficult to achieve in the low impedance pulse line environment.

A NEW DESIGN FOR A CAPACITIVE VOLTAGE MONITOR

It is clear from the brief discussion above that the improvement required for a *D-dot* monitor is to reduce the effect of the intrinsically high coupling capacitance to ground when it is placed in a water line environment. The problem to be solved is to increase the surface area of the tip of the *D-dot* probe while keeping down the capacitive coupling due to the fringing field to the ground electrode. This lead to the present design as shown in Fig.2. The lightly shaded areas are plastic and the grey areas are the probe tip (V-shaped) and the metal body of the monitor. Semi-rigid coaxial cable is used for the output signal connection and is an integral part of the

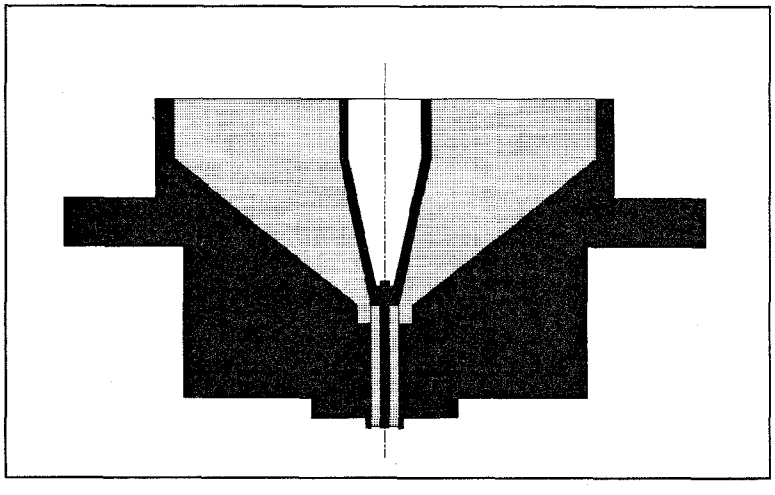

Fig.2 Schematic of the cross-section of the *D-dot* monitor

monitor, shown in black. The idea behind the design is to make the *D-dot* probe body an enlarged but integral section of the signal output cable, with a sufficiently large cross-section at the tip to produce the required coupling capacitance C_L to the live electrode. By extending the 50 Ω cable geometry into the monitor, the intrinsic coupling inductance and capacitance of the connection between the probe and the signal output pick up point is absorbed into the distributed values of a transmission line, which is matched to that of the output signal cable. This design theoretically leads to the optimal high frequency characteristics that can be achieved in practice.

To further reduce the capacitive coupling to the ground electrode, the plastic dielectric between the probe tip and the probe return housing is extended beyond the face of the probe tip and the surrounding ground electrode surface. The low dielectric constant of the plastic compared with that of the water surrounding allows the extended plastic section to function as a field concentrator and to effectively reduce the capacitive coupling to ground. This can be seen from an equipotential plot of the probe as shown in Fig.3. The left hand boundary of this plot is the axis of symmetry and the dark shaded areas are the probe tip electrode and the return ground electrode. The use of a low dielectric constant plastic in a water environment to shape the field distribution was highlighted in a previous work by Sethian[6] on a different application.

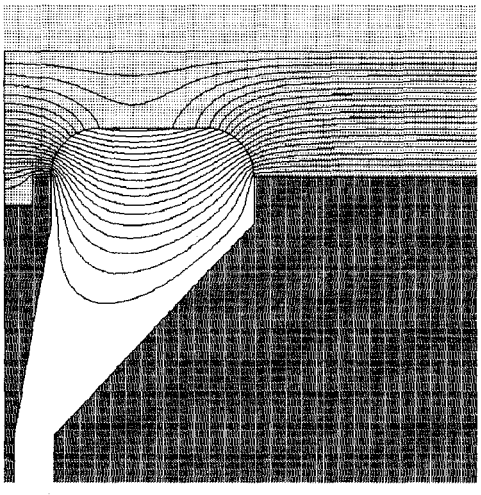

Fig.3 Equipotential plot of a capacitive monitor using the proposed design

This equipotentials distribution can be compared to that from a traditional design, in which water is allowed to penetrate into the region between the probe tip and the return housing. In this case, strong coupling to ground would exist through the water dielectric, with a much higher stray capacitance than in the proposed design. Studies of the equipotential plots of different insulation designs show that the degree of extension of the plastic insulation is not so important when the tip of the probe is expanded to a relatively large diameter as in the present construction.

CIRCUIT SIMULATION

The degree of influence of the stray capacitance to ground was examined using PSpice circuit simulation. A schematic for the practical *D-dot* monitor circuit is shown in Fig.4 with the output taken through a 10 m long transmission line of 50 Ω impedance and terminated with a matched load resistor, followed by a passive integrator at the recording instrument. The design of the monitor here means that no stray inductive component has to be included to the monitor in the circuit schematic. A single voltage pulse of 1 MV, 50 ns duration,

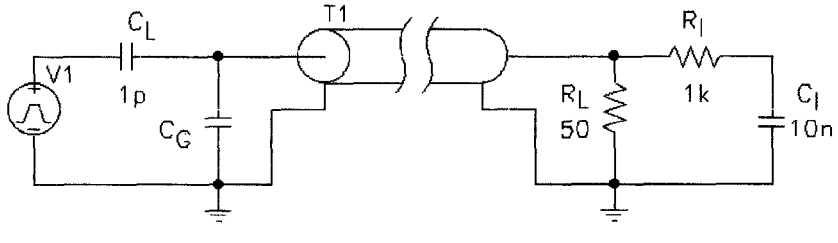

Fig.4 Schematic circuit of the *D-dot* monitor for PSpice simulation

with rise and fall time of 1 ns, was injected through a coupling capacitance C_L of 1 pF. To emulate the experimental condition, a simple RC integrator of 10 μs time constant was used to recover the voltage signal. The circuit was run for different values of C_G , the stray capacitance to ground. The output signal at the load, before and after the integrator, is shown for a range of C_G , from 0.5 pF to 16 pF, in Fig.5. The simulation was run with a maximum time step of 0.25 ns. Only the part relating to the pulse rise time is shown. The low pass effect of the stray inductance can clearly be seen when the value is more than a few pF.

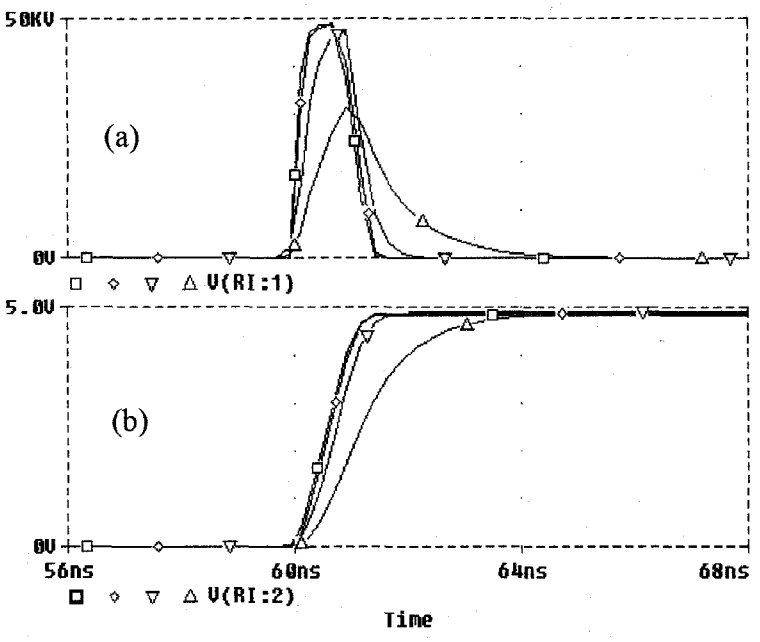

Fig.5 Calculated voltage at the load (a) before the integrator and (b) after the integrator for different values of the stray capacitance to ground. C_G = □ - 0.5 pF, ◇ - 1 pF, ▽ - 4 pF & △ - 16 pF

DISCUSSION

Simple analyses at the beginning of this paper set down the criteria for the *D-dot* & the *Self-integrating* mode of operation of the capacitive monitor. These criteria are not sufficient in terms of the requirement for good high frequency response of the monitor. In particular, the effect of the stray capacitance to ground must be considered and is of great importance when the monitor is used in a high dielectric constant medium. The design of the *D-dot* capacitive monitor presented here removes the constraints of this stray capacitance by providing a transmission line structure all the way from the probe tip to the recording instrument end. The construction is simple and could be easily adapted to different pulsed power machine currently in operation. The very good high frequency response would allow the measured signal to be used in quantitative analyses of the behaviour of a dynamic load, as in a plasma load, where the local measurement of voltage would be difficult. A monitor of this design has been constructed and tested successfully on MAGPIE, the TW pulsed power generator at Imperial College, London.[7]

The tapered transition region of the probe remains the element to be addressed. The length of the geometrical taper will determine the mode structure of the highest frequency component and ultimately set the response time of the probe. Different geometries are being studied at present to properly assess the trade off in the present design.

ACKNOWLEDGEMENT

The work here is supported partly under CEC Contract CI1*-CT92-0053

REFERENCES

[1]M. S. DiCapua, "High Speed Electric Field and Voltage Measurements", in *Fast Electrical and Optical Measurements*, Vol. I, ed. J. E. Thompson and L. H. Luessen (Dordrecht: Martinus Nijhoff), 1986.

[2]R. Hebner, "Electro-Optical Measurement Techniques", in *Fast Electrical and Optical Measurements*, Vol. I, ed. J. E. Thompson and L. H. Luessen (Dordrecht: Martinus Nijhoff), 1986.

[3]C.A. Ekdahl, "Voltage and current sensors for a high density z-pinch experiment", Rev. Sci.Instrum., **51**(12), p. 1645 (1980).

[4]R. Gratton et al., *Rev. Sci. Instrum.*, **57**, p. 2634 (1986).

[5]J.R. Cooper, E.Y. Chu, and R.M. Ness, "An innovative fast-response, co-axial, capacitive high voltage probe", Proc 7th IEEE Pulsed Power Conf., Monterey,CA, 1989, p.390.

[6]J.D. Sethian, "A compact parallel plate water capacitor", Proc 8th IEEE Pulsed Power Conf., San Diego,CA, 1991, p.170.

[7]P.Choi et al, "The MAGPIE programme", Proc 8th IEEE Pulsed Power Conf., San Diego,CA, 1991, p.173.