PONTIFICIA UNIVERSIDAD CATOLICA DE CHILE
SCHOOL OF ENGINEERING

DISCRETE-TIME NOISE FILTERING FOR PULSE-PROCESSING IN PARTICLE PHYSICS EXPERIMENTS

DIEGO ÁVILA GÁRATE

Thesis submitted to the Office of Research and Graduate Studies
in partial fulfillment of the requirements for the degree of
Master of Science in Engineering

Advisor: ÁNGEL ABUSLEME HOFFMAN

Santiago de Chile, July 2014

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ABSTRACT

Particle Physics is the branch of physics that studies the fundamental constituents of matter and radiation, and their mutual interactions. The main tools used by particle physicists are particle accelerators, which use electromagnetic fields to accelerate charged particles to relativistic speeds before they are made to collide inside detectors. The International Linear Collider (ILC), a next generation, 31-kilometer long linear particle accelerator, will smash electron and positron bunches at up to 500 GeV. Located at the ILC detector forward region is the BeamCal, a highly segmented calorimeter detector. The BeamCal specifications for radiation tolerance, noise, signal charge, pulse rate and occupancy pose unique challenges for the instrumentation system.

Framed in the design, integration and testing of the Bean IC, a 5-channel application specific integrated circuit (ASIC) planned to meet the BeamCal instrumentation needs, this thesis presents: the development of a new mathematical framework for a design-oriented analysis of discrete-time filters in the discrete-time domain; and the design and implementation of a switched-capacitor (SC) filter for arbitrary weighting function synthesis to be included in the Bean IC, which aims to take full advantage of the introduced mathematical framework.

Keywords: Charge Measurements, Low-noise filters, Noise, Nuclear Physics Instrumentation, Optimum Digital Filtering.

RESUMEN

La Física de Partículas es la rama de la física que estudia las constituyentes fundamentales de la materia y la radiación, y sus interacciones mutuas. Las principales herramientas utilizadas por los físicos de partículas son los aceleradores de partículas, los cuales usan campos electromagnéticos para acelerar partículas cargadas a velocidades relativistas, para después hacerlas colisionar dentro de detectores. El Colisionador Lineal Internacional (ILC) es un acelerador de partículas lineal de la próxima generación de 31 kilómetros de largo que colisionará grupos de electrones y positrones a 500 GeV. Ubicado en la región delantera del ILC se encuentra el BeamCal, un calorímetro altamente segmentado. Las especificaciones del BeamCal para tolerancia a la radiación, ruido, señal de carga, tasa de pulsos y ocupación plantean desafíos únicos para el sistema de instrumentación.

Enmarcado en el diseño, integración y prueba de *Bean IC*, un circuito integrado de aplicación específica (ASIC, por su sigla en inglés) de cinco canales para satisfacer las necesidades de instrumentación del BeamCal, esta tesis presenta: el desarrollo de un nuevo marco matemático para el análisis orientado al diseño de filtros de tiempo discreto; y el diseño y implementación de un filtro de capacitores conmutados para la síntesis de funciones de peso arbitraria que será incluido en *Bean IC*, el cual busca aprovechar al máximo el marco matemático propuesto.

Palabras Claves: Medición de carga, Filtros de Bajo Ruido, Ruido, Instrumentación para Física Nuclear, Filtrado Digital Optimo.

1. INTRODUCTION

1.1 Particle physics experiments

Particle physics, also called High Energy Physics, is the branch of physics that studies the fundamental constituents of matter and radiation, and their mutual interactions. It aims to answer some of the profound questions of physics, with benefits spanning everything from advancing humankind's understanding of the universe, to applications in other fields of science as well as daily life (Tuttle, 2013).

The main tools used by experimental particle physicists are particle accelerators, which use electromagnetic fields to accelerate charged particles to relativistic speeds before they are made to collide inside detectors. The detectors gather clues about the particles – including their speed, mass and charge – from which physicists can work out a particle's identity (CERN, 2013). An example of such an accelerators is the Large Hadron Collider (LHC) at *Organisation européenne pour la recherche nucléaire* (CERN), which recently proved the existence of the Higgs field (Aad et al., 2012; Chatrchyan et al., 2012), a key element to complete the Standard Model and one of the greatest scientific achievements of the past half-century.

Because experimenters seek ever-increasing high-energy collisions to make new discoveries, and because there are greater discoveries yet to be made, new and larger particle accelerators appear on the roadmap of the scientific community. Up to date, there are two projects in the race to define the LHC's successor, the International Linear Collider (ILC) and the Compact Linear Collider (CLIC), both coordinated by the Linear Collider Collaboration.

As the collision energy increases with each new accelerator generation, so does the complexity of the detectors used to gather information about the collisions. This makes it

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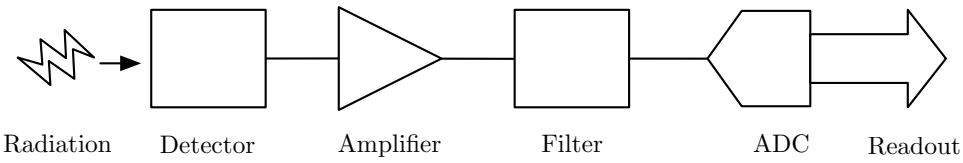

FIGURE 1.1. Block diagram for a single channel, generic instrumentation circuit for particle physics experiments.

necessary a continuous improvement of the techniques used in instrumentation for particle physics. An example of this is the introduction of the CMOS technology in the early 80's, which changed the trend of detector front-end electronics from printed circuit boards (PCBs) to custom integrated circuits, improving integration and allowing on-site electronics with a minimum of mass added to the detector system (Abusleme, 2011).

This thesis deals with an emerging trend to improve the electronics used in particle physics: the use of discrete-time filters to lower the noise present in the detectors front-end circuits. A new mathematical framework for noise analysis of discrete-time filters is presented, in an attempt to guide a proper filter design when a discrete-time filter is used for pulse-processing purposes. Additionally, the design and characterization of a front-end filter for one of the detectors planned for the ILC is presented.

In this chapter, a typical front-end circuit for a detector system is described. Then, current trends for noise minimization in front-end electronics for particle physics experiments are reviewed. Finally, a brief outline of this thesis is presented.

1.2 Electronics for particle physics experiments

A typical particle physics experiment detector system is composed by layer upon layer of complex subdetectors, each of which is usually highly segmented into a multi-channel electrode array. A single channel includes a detector, a preamplifier, a filter, an analog-to-digital converter (ADC), and a readout circuit (Spieler, 2005). Fig. 1.1 shows a highly simplified block diagram of such a detector channel.

The initial amplifier translates the input charge signal, coming from the detector electrodes, into an output voltage signal. Charge-to-voltage conversion is done by transferring the charge Q_{in} from the nonlinear detector capacitance to a linear, known capacitor C. The output voltage is given by $V_{out} = Q_{in}/C$, with C easily selectable and precisely tailorable. Fig. 1.2 depicts the most common preamplifier implementation, which consists of a voltage amplifier with a capacitor in a negative feedback configuration. The resulting circuit is a charge-sensitive amplifier (CSA), extensively studied in the literature (Alvarez, Avila, Campillo, Dragone, & Abusleme, 2012; Aspell et al., 2001; De Geronimo & O'Connor, 2005; O'Connor & De Geronimo, 1999; Snoeys, Campbell, Heijne, & Marchioro, 2000). The amplified signal includes noise from the detector and the CSA. Since the noise statistics are well modeled, they can be used to design a filter that maximizes the signal-to-noise ratio (SNR) at the detector front-end output. Usually the filter is an analog block, either time-invariant or time-varying, used to convert the voltage signal at the CSA output into a shaped voltage pulse. The pulse shape defines the weights of noise sources on the front-end output noise. Thus, a proper selection of the pulse shape is part of the solution to the SNR maximization problem. A memory acts as a buffer necessary to store data for a number of events before readout. For high-frequency pulse trains, analog memory is particularly well suited (Haller & Wooley, 1994; Kleinfelder, Chen, Kwiatkowski, & Shah, 2004). Filtered signals can be quickly stored as charge in integrated capacitors, to be converted into digital signals by dedicated ADCs during the readout phase. Integration and feature size reduction has allowed the design of highly dense digital memory arrays. If a digital memory is used instead, ADCs are used to digitize the signal prior to storage, and conversion throughput per IC must be as high as the collision rate times the number of channels.

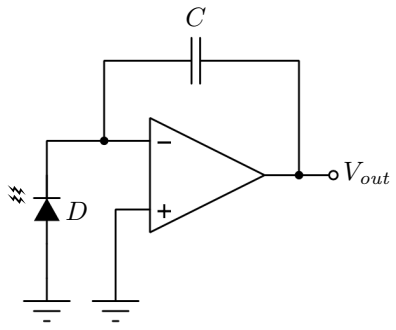

FIGURE 1.2. CSA using a voltage amplifier. Detector is modeled as a photodiode.

1.3 Noise minimization in circuits for particle physics instrumentation

1.3.1 Basic notions

Noise, in the broadest sense, can be defined as any unwanted disturbance that obscures or interferes with a desired signal (Motchenbacher & Fitchen, 1973). In electronics, noise is a random fluctuation that results from the physics of the devices and materials that make up the electrical system. It represents an important issue in the design of integrated circuits, since it determines the smallest signal level that can be processed on any real circuit. Noise generated by electronic devices, such as field-effect transistors and bipolar transistors, varies widely, as the operation of these devices involves several different physical processes, with many of them prone to spontaneous fluctuations. There are three sources of fundamental noise in MOSFETs (Gray, Hurst, Lewis, & Meyer, 2001): shot noise due to gate leakage current, thermal (for strong inversion operation) or shot (for weak inversion operation) noise in the channel, which is always white noise, and flicker or $1/f$ noise, also called pink noise. These noise sources have been extensively studied over the years, and several works about them can be found in the literature. References (Gray et al., 2001; Jindal, 2006) are good starting points for introducing the reader into this subject.

As most times noise is assumed to be a stationary stochastic process, it is natural to study it in the frequency domain, where it is commonly expressed as a noise power spectral density. The integral of the noise power spectrum over the circuit bandwidth yields the total circuit noise power, and its square root is the standard deviation.

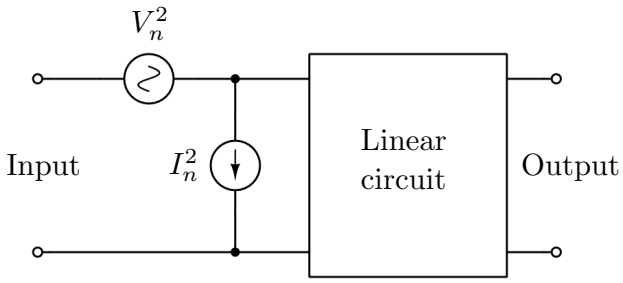

FIGURE 1.3. Equivalent representation of a linear circuit internal noise sources referred to the input port.

In an electronic circuit, composed by a number of electronic devices, there are several noise sources. To quantitatively compare the effect of these noise sources, each one of them can be referred to a common node of the circuit, typically the input node. Noise sources referred to the same circuit node are added up as follows:

$$\sigma_{Total}^2 = \sum_{i=1}^{N} \sigma_i^2 + \sum_{i \neq j} c_{i,j} \cdot \sigma_i \cdot \sigma_j \tag{1.1}$$

where σ_i^2 represents the noise power of source i, N is the number of noise sources, and $c_{i,j}$ is the correlation coefficient between two noise sources.

By referring the noise sources to the input of the circuit, it is possible to make a fair comparison of noise performance among different circuits with common application, and set the total input-referred noise as a figure of merit. In a linear circuit, the total input-referred noise can be represented by a combination of a series voltage noise source (V_n^2) and a parallel current noise source (I_n^2), as shown in Fig. 1.3. If the driving signal is a low-impedance voltage source, the voltage noise is dominant and the current noise can be neglected, whereas if the signal source is a high-impedance current source, the voltage noise can be neglected, as current noise accounts for all the circuit noise. In circuits with a non-ideal load line, both noise sources must be considered.

1.3.2 Noise minimization in particle physics instrumentation systems

In general, on any signal processing system, noise minimization is carried out through a careful design of the first processing stages, which for particle physics experiments corresponds to the detector front-end circuit, and specifically, the detector electrodes, the CSA and the pulse-shaper. Understanding and designing for low noise has been one of the main concerns in modern particle physics instrumentation. Any survey on this topic starts with a work published in 1968 (Radeka, 1968), where important concepts of pulse shaping for particle physics experiments were described as well as introduced. Among these is the weighting function (WF) concept, a time-domain representation of the total integrated noise, a useful tool to calculate the noise of a typical detector front-end circuit, which is still in use nowadays.

In 1972, a design-oriented time-domain analysis based on the WF concept was published (Goulding, 1972). In this work it was demonstrated that, assuming only white noise, all the noise sources in a detector front-end circuit can be reduced to two noise sources at the input node: a parallel noise source and a series noise source. Integration of each component in frequency yields two noise coefficients that make it possible to characterize the noise-filtering capabilities of a pulse shaper.

In 1988, results from previous works on noise were summarized in one of the most influential papers in low-noise techniques for particle physics instrumentation (Radeka, 1988). The formalization and stringency of this work guided the subsequent work on the field.

Study of flicker noise in particle physics electronics was introduced in (Lutz, Manfredi, Re, & Speziali, 1989). Before this work, flicker noise was almost never considered in the design for particle physics electronics. In 1990, the problem of finding the optimum WF for particle physics electronics, including flicker noise in the analysis, was published (Gatti, Sampietro, & Manfredi, 1990). The same year, an excellent derivation of noise for particle physics front-end electronics, including thermal, flicker and shot noise sources was presented (Sansen & Chang, 1990).

In (Gadomski et al., 1992), the deconvolution method for pulse-shaping was presented. Major innovations of this work come from the use of switched-capacitor filters for pulse-processing purposes and the introduction of the concept of discrete-time pulse-shaping.

In (Pullia, 1998), for the first time the flicker noise is analyzed in the time domain. A generalization of this work was presented in (Pullia & Riboldi, 2004), allowing time-domain simulations of almost all kind of noise sources. This work represents a powerful tool for computer-aided filter design.

Finally, excellent books on particle physics instrumentation systems have been published (Radeka, 2011), compiling and explaining the results from many papers in the field.

1.4 Thesis content

Chapter 2 starts with an introduction to the project that prompts the work of this thesis, the design and implementation of a second iteration of the Bean, an instrumentation application-specific integrated circuit (ASIC) which forms part of the proposal for the ILC. It is followed by an overview of the motivations that led to the development of a new mathematical framework for noise analysis in discrete-time filters, alongside with the presentation of the requirements for a filter intended to take full advantage of this framework. Chapter 3 presents the complete formulation of this noise analysis, including examples and applications for optimal filter computation. In Chapter 4 , the design and implementation of a filter for arbitrary weighting function synthesis are presented. Chapter 5 shows the results that contribute to the ongoing project, functionality verifications of the designed filter and the implementation of an early prototype of the Bean V2, with the filter as one of its core building blocks. Finally, Chapter 6 summarizes the results and contributions of this work, and presents ideas for future research.

2. PROBLEM DEFINITION

2.1 The BeamCal Instrumentation

The work described in this thesis is a contribution to the design and implementation of the front-end circuit for one of the detector systems of the International Linear Collider (ILC). The project is endorsed by the ILC Forward Calorimetry Collaboration (FCAL), a worldwide detector research and development collaboration, and party sponsored by CONICYT through the FONDECYT Program.

Planned to be operating in the mid 2020's, the ILC will be the largest linear particle collider ever built. Consisting of two linear accelerators that will stretch approximately 32 kilometers in length, the ILC will smash electrons and positrons together at nearly the speed of light. The intended beam collision energy is 500 billion-electron-volts (GeV) for the first stage, with the possibility for a later upgrade to 1 TeV.

Located at the ILC detector forward region, the BeamCal is a highly segmented ($>$ 90000 channels) calorimeter that will serve four main purposes: improve the hermeticity of the ILC detector for low polar angles, reduce the backscattering from pairs into the inner ILC detector part, protect the final magnet of the beam delivery system, and assist the beam diagnostics. The BeamCal specifications for radiation tolerance, noise, signal charge, pulse rate and occupancy pose unique challenges for the instrumentation system. Although initially planned for the ILC, the BeamCal calorimeter could also be used in the Compact Linear Collider (CLIC), the alternative particle accelerator in race to follow the LHC.

The FONDECYT project #11110165: Application of Advanced CMOS Techniques in Pulse Processors for Particle Physics Experiments deals with the design and implementation of a mixed-signal application-specific integrated circuit (ASIC) to address the BeamCal instrumentation needs. The IC, called the Bean, will be designed for a standard 180-nm CMOS process and will be based on a 3-channel prototype developed in a

previous work (Abusleme, Dragone, Haller, & Wooley, 2012). Each independent channel will include: a charge-sensing amplifier with a pre-charging pulser; a fully differential switched-capacitor (SC) filter with a low-frequency noise suppression feature; a 10-bit, fully-differential, successive approximation register (SAR) charge redistribution analog-to-digital converter (ADC); and a digital storage array. Additionally, the IC will feature a fast feedback adder for beam diagnostics purposes. Fig. 2.1 shows a block diagram of a prototype version of the Bean, which does not include the digital storage array nor the nominal number of channels. The IC will be capable of processing the BeamCal detector output at the ILC nominal frequency of $3.2468\,\text{MHz}$, with 100% occupancy[1]. Also, each channel must be able to deal with two different modes of operation: the standard data taking (SDT) mode, and the detector calibration (DCal) mode. According to the actual BeamCal specifications, the maximum input signals were to be about 37 pC in the SDT mode, and 50 times smaller in the DCal mode. Table 2.1 summarizes the BeamCal instrumentation ASIC specifications.

Beyond the purpose of addressing the BeamCal instrumentation needs, the general goal of this project is to prove that advanced CMOS circuit design techniques, such as SC circuits and ADCs based on MOM capacitors, can be used effectively to address the instrumentation requirements in particle physics experiments. The specific goals of this project to be covered by this thesis are:

1. to achieve a thorough understanding of the noise of SC filters in particle physics experiments, and
2. to prove the successful synthesis of arbitrary WFs by means of SC circuits.

The first goal is sorted out with the development of a mathematical framework for noise analysis in discrete-time filters presented on Chapter 3, which is not only suited for SC filters, but for any discrete-time block introduced on the signal path of the circuit in analysis.

[1] Occupancy is the fraction of channels that register a relevant stimulus on each collision.

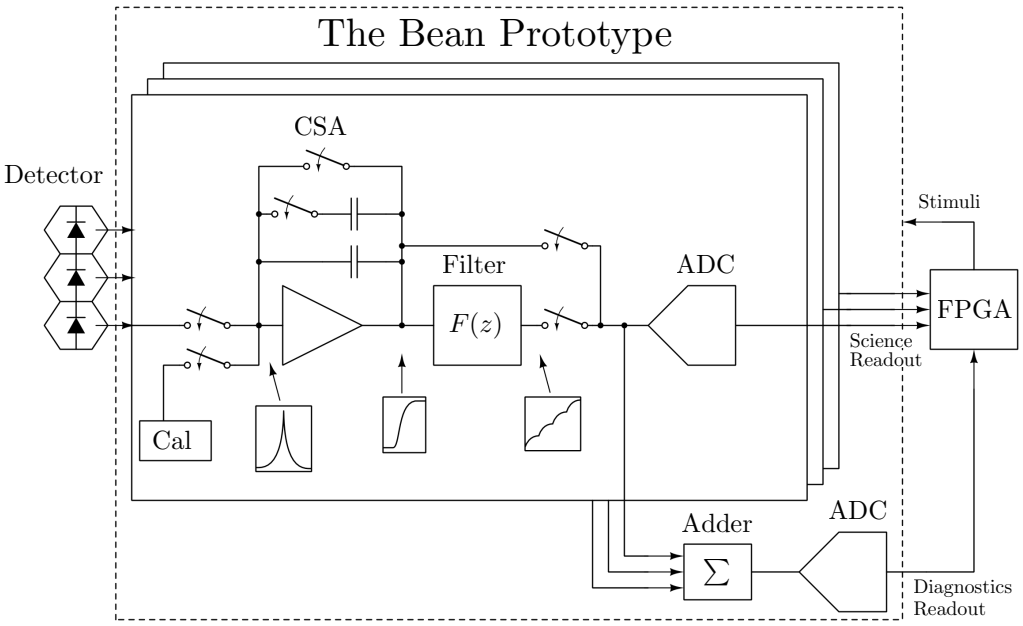

FIGURE 2.1. The Bean prototype block diagram.

Input rate	3.25 MHz during 0.87 ms, repeated every 200 ms
Channels per ASIC	32
Occupancy	100%
Resolution	10 bits for individual channels, 8 bits for fast feedback
Modes of operation	Standard data taking (SDT), Detector Calibration (DCal)
Input signals	Up to 40 pC in SDT, 0.74 pC in DCal
Input capacitance	65 pF
Additional feature	Low-latency (1 μs) output
Additional feature	Internal pulser for electronics calibration
Radiation tolerance	1 Mrad (SiO_2) total ionizing dose
Power consumption	2.19 mW per channel
Total ASIC count	2836

TABLE 2.1. BeamCal instrumentation ASIC specifications summary.

The second goal is carried out by means of the implementation of the front-end filter for the Bean, which development is shown in Chapter 4.

3. NOISE ANALYSIS IN PULSE-PROCESSING DISCRETE-TIME FILTERS[1]

3.1 Introduction

In particle physics experiments, where the results from the collisions are inferred from the measurement of electric charge in various sets of detectors (Gatti & Manfredi, 1986; Radeka, 1988), noise sets a fundamental limit for the charge measurement resolution (Geronimo, O'Connor, Radeka, & Yu, 2001). In such experiments, the typical detector front-end circuit comprises a charge-sensitive amplifier (CSA) and a filter, often referred to as pulse shaper. The former is used to convert the input charge signal, coming from the detector electrodes, into a voltage signal, and is responsible for most of the noise present in the readout circuit signal path (De Geronimo & O'Connor, 2005; Geronimo et al., 2001). The filter is used to convert the voltage signal at the CSA output into a shaped voltage pulse, in order to maximize the signal-to-noise ratio (SNR) at the measurement time.

Different noise analysis methods have been proposed to guide a proper filter design. The outcome of these methods is the equivalent noise charge (ENC), a measure of the front-end noise defined as the charge required at the detector input to produce an output SNR of 1. A time-domain analysis based on the weighting function (WF) concept (Goulding, 1972; Radeka, 1988) has long been the preferred analysis, since it allows to find the optimum filter for a wide range of detector configurations (Gatti, Geraci, & Ripamonti, 1996; Geraci & Gatti, 1995; Pullia, 1997; Pullia & Gatti, 2002; Radeka, 1968).

Traditionally, the filter synthesis has been performed using continuous-time networks. However, since producing arbitrary WFs by means of continuous-time analog circuitry is often impossible (Gatti et al., 1996), this approach does not always allow to synthesize optimum filters. A different approach based on discrete-time filters, implemented by means of digital signal processor (DSP) units (Geraci, Zambusi, & Ripamonti, 1996;

[1] See also (Avila, Alvarez, & Abusleme, 2013).

Jordanov, 2003; Sampietro, Bertuccio, Geraci, & Fazzi, 1995) or switched capacitor networks (Abusleme et al., 2012; Fiorini & Buttler, 2002; Porro, Herrmann, & Hornel, 2007), allows to synthesize WFs with virtually any shape, producing near-optimum filters. Moreover, this promising approach takes advantage of the aggressive technology scaling and the new techniques of the VLSI industry, allowing to implement fast, reliable and flexible filters.

In this work, a mathematical framework for a design-oriented analysis of discrete-time filters in the discrete-time domain is presented. Although discrete-time filters can be analyzed using a continuous-time method, it is not insightful and the resulting expressions are complex and difficult to use for design purposes. Furthermore, the analysis of discrete-time filters in the discrete-time domain provides a better insight on how their discrete nature affects the front-end noise. The proposed analysis can produce closed-form expressions for the ENC calculation, which can be used for efficient algorithms for the ENC evaluation and filter optimization procedures.

In order to validate the proposed framework in this work, an example is developed, and the result obtained is analyzed and compared with the result provided by the continuous-time approach. Also, an example of optimal filter computation is presented to demonstrate the capabilities of the proposed framework.

3.2 Discrete-Time Analysis

Figure 3.1 shows a simplified model to compute the output-referred noise contribution of a single noise source in a typical front-end detector. It consists of a linear block with a transfer function $H(s)$ that models the effect of the CSA on the noise source under analysis, and a pulse shaper, which in this case is a finite impulse response (FIR) filter with a discrete-time transfer function given by

$$F(z) = \sum_{j=0}^{N-1} a_{N-j}\, z^{-j} \tag{3.1}$$

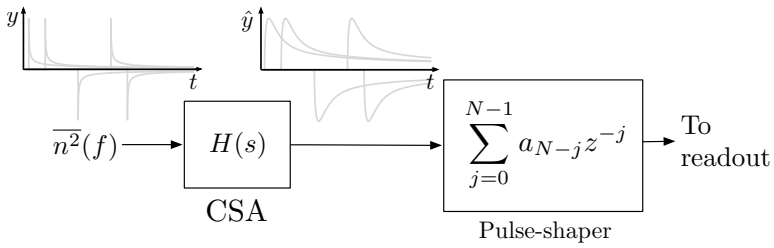

FIGURE 3.1. Model for noise analysis in a typical front-end circuit.

where a_{N-j} are arbitrary coefficients and N is the filter length. The noise source is characterized by its two-sided power spectral density (PSD) $\overline{n^2}(f)$.

For this analysis it is not necessary to consider the details of the physical processes that cause the noise. It will be assumed that the noise source is an arbitrary white or filtered white noise source, which represents any of the fundamental noise sources present at a detector front-end circuit, such as thermal noise, shot noise and flicker noise. This assumption allows to model the noise source in the time domain in terms of a sequence of noise pulses with core function $y(t)$, arriving Poissonianly at times t_a with an average rate ν and random sign (Goulding, 1972; Radeka, 1988). A general procedure to calculate a function $y(t)$ that represents the noise process characterized by $\overline{n^2}(f)$ can be found in (Pullia & Riboldi, 2004).

By using the CSA transfer function and $y(t)$, the effect of an individual noise pulse at the filter input can be determined as

$$\hat{y}(t) = y(t) * \mathcal{L}^{-1}\{H(s)\}(t). \tag{3.2}$$

Both sequences of pulses, at the input and at the output of $H(s)$, are illustrated in Figure 3.1.

Assuming a periodic, synchronous front-end, where the stimulus arrival time within each frame is fixed and known, the CSA can be reset at the beginning of each frame, prior to the corresponding stimulus. Thus, the analysis can be carried out considering a non-stationary noise process that starts at $t = 0$. Then the total integrated noise at the filter input is a function of time (Radeka, 2011). Using (3.2) and Campbell's theorem, the

following expression for the total integrated noise at the filter input can be derived:

$$\sigma^2(t) = \nu \int_0^t \hat{y}^2(t - t_a)\ \mathrm{d}t_a. \tag{3.3}$$

Let us define P_i as the time interval between an arbitrary sample i and its predecessor, given by $P_i = [(i-1)T_s, iT_s]$, where T_s is the filter sampling period. Now consider the noise contribution of the pulses originated within P_i and measured at an arbitrary sample k (i.e., $t = kT_s$), $\sigma_i^2(k)$, as shown in Figure 3.2. Using Campbell's theorem, $\sigma_i^2(k)$ can be computed as

$$\sigma_i^2(k) = \nu \int_{(i-1)T_s}^{iT_s} \hat{y}^2(kT_s - t_a)\ \mathrm{d}t_a\,. \tag{3.4}$$

It can be shown that (3.4), can be expressed as

$$\sigma_i^2(k) = \int_0^{T_s} \hat{y}^2\left(\left(k - i + 1\right) T_s - \eta_1\right)\ \mathrm{d}\eta_1 \tag{3.5}$$

where $\eta_1 = t_a + T_s - iT_s$. This integral can be split into two integrals as follows

$$\begin{aligned} \sigma_i^2(k) = & \int_0^{(k-i+1)T_s} \hat{y}^2\left(\left(k - i + 1\right) T_s - \eta_1\right)\ \mathrm{d}\eta_1 \\ & - \int_{T_s}^{(k-i+1)T_s} \hat{y}^2\left(\left(k - i + 1\right) T_s - \eta_2\right)\ \mathrm{d}\eta_2. \end{aligned} \tag{3.6}$$

Defining $\eta_2 = \eta_3 + T_s$, (3.6) can be written as

$$\begin{aligned} \sigma_i^2(k) \ = \ & \int_0^{(k-i+1)T_s} \hat{y}^2\left(\left(k - i + 1\right) T_s - \eta_1\right)\ \mathrm{d}\eta_1 \\ & - \int_0^{(k-i)T_s} \hat{y}^2\left(\left(k - i\right) T_s - \eta_3\right)\ \mathrm{d}\eta_3. \end{aligned} \tag{3.7}$$

Since $\hat{y}^2(t)$ is zero for negative arguments, then $\sigma_i^2(k) = 0$ for $k < i$. For $k \geq i$, and according to (3.3), (3.7) can be alternatively expressed as

$$\sigma_i^2(k) = \sigma^2\left(\left(k - i + 1\right) T_s\right) - \sigma^2\left(\left(k - i\right) T_s\right) \tag{3.8}$$

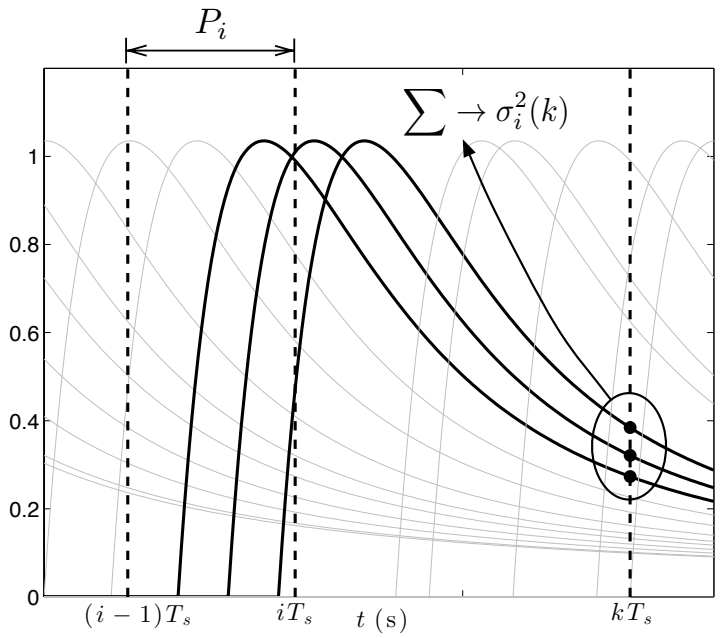

FIGURE 3.2. Noise contribution of the pulses generated within P_i and measured at an arbitrary sample k (i.e., $t = kT_s$), using an arbitrary filtered noise core function $\hat{y}(t)$. The independent contribution of each pulse is pointed out with black dots.

therefore,

$$\sigma_i^2(k) = \begin{cases} \sigma^2((k-i+1)T_s) - \sigma^2((k-i)T_s), & k \geq i \\ 0, & k < i. \end{cases} \tag{3.9}$$

Based on (3.9), the total integrated noise at the filter input measured at the k-th sample, $\sigma^2(kT_s)$, can be written as the sum of the individual noise contributions originated at each interval P_i:

$$\sigma^2(kT_s) = \sum_{i=1}^{N} \sigma_i^2(k). \tag{3.10}$$

The evolution of the total integrated noise at the filter input according to (3.10) is illustrated in Figure 3.3.

Since (3.10) is composed by noise contributions originated at different time intervals P_i, the total integrated noise at the filter input holds partial correlation between samples, and the output noise cannot be computed by convolving (3.10) with $F(z)$. However, since all evaluations of $\sigma_i^2(k)$ are originated from the same pulses (for a fixed i), and thus are fully correlated, (3.10) can be split into N independent discrete-time signals $\sigma_1^2(k), \sigma_2^2(k) \dots \sigma_N^2(k)$. Each of these signals can be referred to the filter output as

$$\begin{aligned}\hat{\sigma}_i(k) &= \sqrt{\sigma_i^2(k)} * \mathcal{Z}^{-1}\{F(z)\}(k) \\ &= \sum_{j=0}^{k-i} a_{N-j} \sqrt{\sigma_i^2(k-j)}. \end{aligned} \tag{3.11}$$

Signals $\hat{\sigma}_1(k), \hat{\sigma}_2(k) \dots \hat{\sigma}_N(k)$ are also independent, and can be added up as noise variances to compute the total integrated noise at the filter output as a function of k:

$$\begin{aligned}\hat{\sigma}^2(k) &= \sum_{i=1}^{k} \hat{\sigma}_i^2(k) \\ &= \sum_{i=1}^{k} \left(\sum_{j=0}^{k-i} a_{N-j} \sqrt{\sigma_i^2(k-j)} \right)^2. \end{aligned} \tag{3.12}$$

Evaluating (3.12) at the measurement time $t_m = NT_s$ (i.e., $k = N$) yields

$$\hat{\sigma}^2(N) = \sum_{i=1}^{N} \left(\sum_{j=0}^{N-i} a_{N-j} \sqrt{\sigma_i^2(N-j)} \right)^2. \tag{3.13}$$

Finally, replacing (3.9) in (3.13) and defining $h = N - j - i$, a closed-form expression for the front-end noise can be obtained:

$$\hat{\sigma}^2(N) = \sum_{i=1}^{N} \left(\sum_{h=0}^{N-i} a_{i+h} \sqrt{\sigma^2((h+1)T_s) - \sigma^2(hT_s)} \right)^2. \tag{3.14}$$

The only term of (3.14) that depends on the input-referred noise process is $\sigma^2(t)$, which can be calculated analytically or numerically for typical noise processes by using (3.3). For instance, Figure 3.4 illustrates $\sigma^2(t)$ for thermal, shot and flicker noise. Even

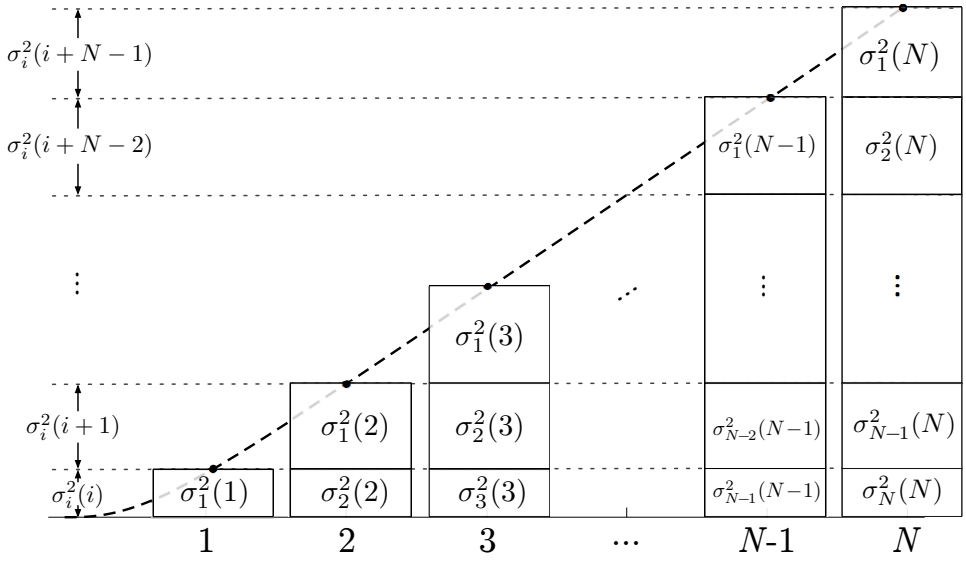

FIGURE 3.3. Evolution of the total integrated noise at the filter input, where the noise of each sample was split according to (3.10).

though the analysis presented here has been applied for a single noise source, it can be easily extended for circuits with several noise sources by applying the superposition principle in quadrature.

3.3 Example

For validation purposes, the thermal noise contribution at the output of a discrete-time integrator filter will be computed using the proposed discrete-time analysis. The result obtained will be analyzed and then compared with the result produced by the traditional continuous-time approach. Figure 3.5 shows the front-end circuit used for general noise analysis. The detector is modeled as capacitance C_D, whereas the CSA is shown as a voltage amplifier with open loop gain $A(s) = A/(1 + s\tau)$, input capacitance C_{in} and a feedback capacitor C_F. Resistor R_R across the feedback capacitor C_F represents the CSA reset element. The filter coefficients are $a_i = 1$. The detector shot noise represented by $\overline{i_D^2}$ will be omitted for the purpose of this example. Thermal noise has been assumed to be dominated by the CSA input device and is represented by two fully-correlated noise

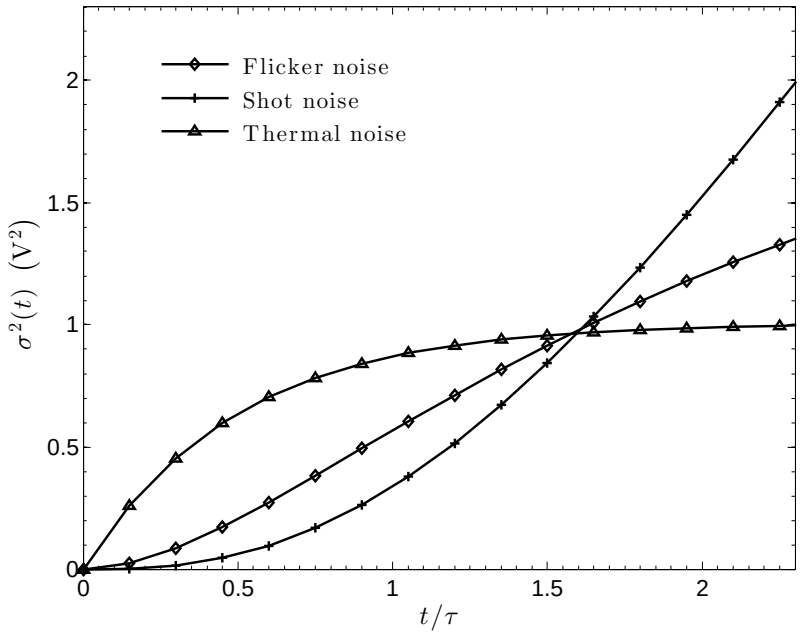

FIGURE 3.4. $\sigma^2(t)$ for thermal, shot and flicker noise with normalized time t/τ and an arbitrary amplitude.

sources (Sansen & Chang, 1990), a voltage white noise source with a two-sided PSD $\overline{v_n^2}$ and a current noise source with a two-sided PSD $\overline{i_n^2}$. Both noise sources are related as follows:

$$\overline{i_n^2} = (sC_{in})^2\,\overline{v_n^2}. \tag{3.15}$$

Considering that the effect of the reset switch during the relatively short time that it takes the CSA to produce an output voltage is negligible, R_R can be assumed to be infinite (Pullia & Riboldi, 2004). The CSA open loop DC gain (A) is assumed to be very large as well. Under these assumptions and using (3.15), the PSD of the thermal noise referred to the CSA output, $\overline{v_o^2}$, can be approximated to

$$\overline{v_o^2} \approx \left|\frac{C_{tot}}{C_f}\frac{1}{1+s\hat{\tau}}\right|^2 \overline{v_n^2} \tag{3.16}$$

where $C_{tot} = C_D + C_F + C_{in}$ and $\hat{\tau} = (\tau/A)(\,C_{tot}/C_f)$ is the CSA closed-loop time-constant.

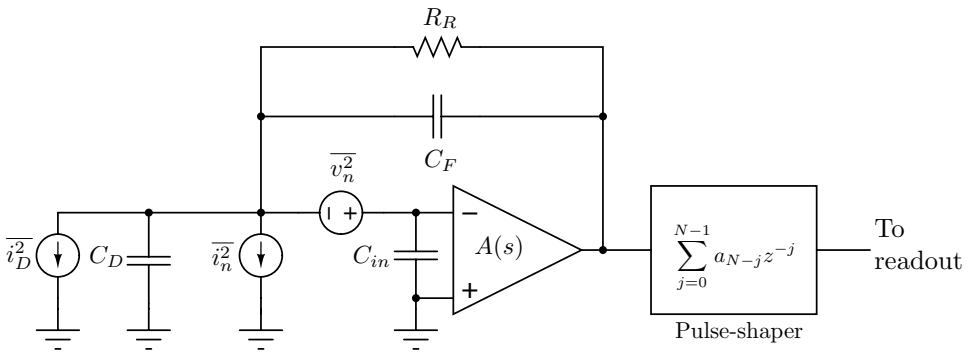

FIGURE 3.5. Front-end circuit used for noise analysis.

The PSD in (3.16) can be treated as the result of passing a fictitious noise source with PSD $\overline{v_n^2}$ through a block with transfer function $H_{\text{th}}(s)$ given by

$$H_{\text{th}}(s) = \frac{C_{tot}}{C_f} \frac{1}{1 + s\hat{\tau}}. \tag{3.17}$$

Since $\overline{v_n^2}$ characterizes a white noise source, it can be modeled as a sequence of Dirac impulses with core function $y_{\text{th}}(t)$ occurring at an arbitrary rate ν and random sign (Pullia & Riboldi, 2004), where $y_{\text{th}}(t)$ is given by

$$y_{\text{th}}(t) = \sqrt{\frac{\overline{v_n^2}}{\nu}} \delta(t). \tag{3.18}$$

Replacing (3.17) and (3.18) in (3.2), each pulse in the sequence can be referred to the CSA output as an exponentially decaying pulse (Pullia & Riboldi, 2004) as follows

$$\hat{y}_{\text{th}}(t - t_a) = \sqrt{\frac{\overline{v_n^2}}{\nu}} \frac{C_{tot}}{C_F} \frac{e^{-(t-t_a)/\hat{\tau}}}{\hat{\tau}} u(t - t_a) \tag{3.19}$$

where $u(t)$ is the unit step function. Substituting (3.19) in (3.3), the filter input total integrated noise due to the thermal noise, $\sigma_{\text{th}}^2(t)$, can be derived:

$$\sigma_{\text{th}}^2(t) = \overline{v_n^2} \frac{C_{tot}^2}{C_F^2} \frac{1 - e^{-2t/\hat{\tau}}}{2\hat{\tau}} u(t). \tag{3.20}$$

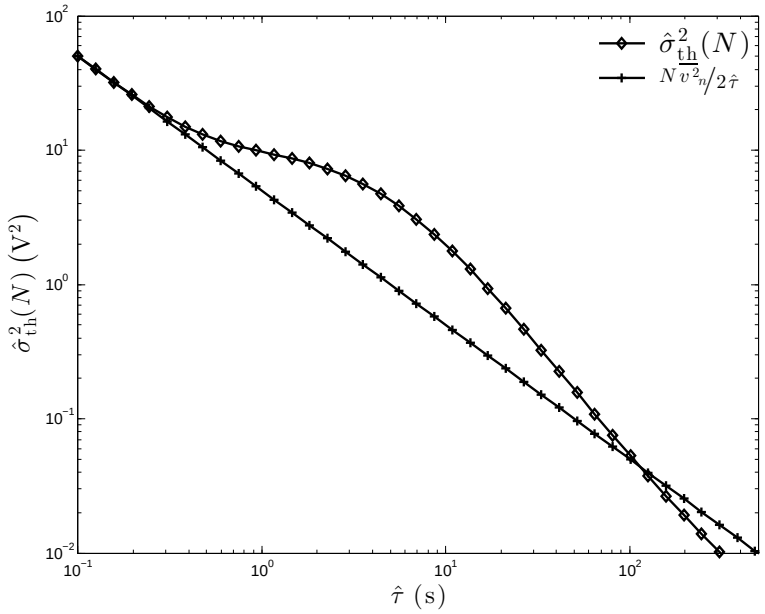

FIGURE 3.6. $\hat{\sigma}^2_{\text{th}}(N)$ and $N\frac{\overline{v_n^2}}{2\hat{\tau}}\frac{C_{tot}^2}{C_F^2}$ as a function of $\hat{\tau}$, using $\overline{v_n^2}=1, C_{tot}^2/C_F^2=1$ and $N=20$.

Finally, replacing (3.20) in (3.14) and defining $x=e^{T_s/\hat{\tau}}$, the front-end noise, $\hat{\sigma}^2_{\text{th}}(N)$, can be obtained:

$$\hat{\sigma}^2_{\text{th}}(N)=\frac{\overline{v_n^2}}{2\hat{\tau}}\frac{C_{tot}^2}{C_F^2}\frac{\left(N(x^2-1)-2x-x^{-2N}+2x^{-N}+2x^{1-N}-1\right)}{(x-1)^2}. \tag{3.21}$$

When the time interval between samples is large enough to consider that consecutive noise samples are uncorrelated (i.e., $\hat{\tau}\ll T_s$), $\hat{\sigma}^2_{\text{th}}(N)$ can be approximated without the use of the proposed analysis as a weighted sum of the uncorrelated samples of the total integrated noise at the CSA output as follows:

$$\hat{\sigma}^2_{\text{th}}(N)\big|_{\hat{\tau}\ll T_s}\approx N\lim_{t\to\infty}\sigma^2(t)=N\frac{\overline{v_n^2}}{2\hat{\tau}}\frac{C_{tot}^2}{C_F^2}. \tag{3.22}$$

As shown in Figure 3.6, (3.21) behaves as predicted by (3.22) for small values of $\hat{\tau}$.

Now, the same example will be analyzed using the traditional continuous-time approach. Using (3.19), the WF $w(t)$, defined as the contribution of each pulse occurring at

time t measured at a fixed time $t_m = NT_s$ at the output of the filter, is given by

$$\begin{aligned} w(t) &= \sum_{n=1}^{N} \hat{y}_{\text{th}}(nT_s - t) \\ &= \sqrt{\frac{\overline{v_n^2}}{\nu}} \frac{C_{tot}}{C_F} \sum_{n=1}^{N} \frac{e^{-(nT_s - t)/\hat{\tau}}}{\hat{\tau}} u(nT_s - t). \end{aligned} \tag{3.23}$$

Integrating (3.23) from the reset time ($t = 0$) to the signal measurement time ($t = t_m$), the filter total integrated noise at $t = t_m$ can be computed as

$$\begin{aligned} \hat{\sigma}_{\text{th}}^2(N) &= \nu \int_0^{t_m} w^2(t)\, \mathrm{d}t \\ &= \overline{v_n^2} \frac{C_{tot}^2}{C_F^2} \int_0^{NT_s} \left(\sum_{n=1}^{N} \frac{e^{-(nT_s - t)/\hat{\tau}}}{\hat{\tau}} u(nT_s - t) \right)^2 \mathrm{d}t. \end{aligned} \tag{3.24}$$

Defining $\alpha = T_s/\hat{\tau}$ and $\beta = t/\hat{\tau}$, (3.24) can be re-written as

$$\hat{\sigma}_{\text{th}}^2(N) = \frac{\overline{v_n^2}}{\hat{\tau}} \frac{C_{tot}^2}{C_F^2} \int_0^{N\alpha} e^{2\beta} \left(\sum_{n=1}^{N} e^{-n\alpha} u\left(n\alpha - \beta\right) \right)^2 \mathrm{d}\beta \tag{3.25}$$

which can be split into a sum of integrals as follows

$$\hat{\sigma}_{\text{th}}^2(N) = \frac{\overline{v_n^2}}{\hat{\tau}} \frac{C_{tot}^2}{C_F^2} \sum_{n=1}^{N} \int_{(n-1)\alpha}^{n\alpha} e^{2\beta} \left(\sum_{k=n}^{N} e^{-k\alpha} \right)^2 \mathrm{d}\beta. \tag{3.26}$$

Finally, defining $x = e^{\alpha}$ it can be shown that (3.26) is equal to (3.21).

3.4 ENC Minimization

For filter optimization purposes, a typical front-end circuit with thermal, shot and flicker noise components is considered. The front-end configuration from Figure 3.5 will be used. In this case, the pulse shaper is a discrete-time FIR filter with indeterminate coefficients a_i. Shot noise is assumed to be dominated by the detector noise and is represented by a white noise current source with two-sided PSD $\overline{i_D^2}$ in parallel with the detector capacitance C_D and given by

$$\overline{i_D^2} = qI_L \tag{3.27}$$

where q is the electron charge and I_L the detector leakage current. Thermal noise and flicker noise are assumed to be dominated by the noise of the CSA input device and are represented by two fully-correlated noise sources, a voltage noise source with two-sided PSD $\overline{v_n^2}$ given by

$$\overline{v_n^2} = a_T + \frac{a_F}{|f|} \tag{3.28}$$

where a_T and a_F are the thermal and flicker coefficients, and a current noise source with two-side PSD $\overline{i_n^2}$ given by (3.15). Traditionally, the coefficients a_T and a_F are obtained from the CSA input device models. However, for design purposes the most accurate values shall be used, and these coefficients should be extracted from experiments (Bertuccio & Pullia, 1993) or precise simulations.

Considering the contribution of each noise process separately, the ENC^2 for the output measured at $t = NT_s$ can be written as

$$ENC^2 = \frac{\hat{\sigma}^2_{\text{shot}}(N) + \hat{\sigma}^2_{\text{th}}(N) + \hat{\sigma}^2_{1/f}(N)}{q^2 \left|\max[w(t)]\right|^2 / C_F^2} \tag{3.29}$$

where $\hat{\sigma}^2_{\text{shot}}(N)$ is the shot noise contribution, $\hat{\sigma}^2_{\text{th}}(N)$ is the thermal noise contribution, $\hat{\sigma}^2_{1/f}(N)$ is the flicker noise contribution and $w(t)$ is the weighting function at the front-end output given by (3.23).

In order to find the coefficients a_i that minimize (3.29), and hence the optimal FIR filter, the signal measurement time $t_m = NT_s$ was assumed to be a constant determined by the processing time budget constraints, and the filter sampling period T_s was assumed to be a constant determined by the filter maximum clock rate. Although $\hat{\tau}$ is a design variable that depends on the CSA and not on the filter, it has been included in the optimization analysis.

Given that a common WF reaches its maximum value at $t = t_m/2$, and that the WF height is commonly a design constraint, the denominator of (3.29) was forced to be constant by fixing the WF height, h_w, through the following constraints

$$\sum_{i=1}^{N/2} a_i \left(1 - e^{-T_s(N/2-i+1)/\hat{\tau}}\right) = h_w \tag{3.30}$$

$$\sum_{i=1}^{N} a_i \left(1 - e^{-T_s(N-i+1)/\hat{\tau}}\right) = 0. \tag{3.31}$$

Although these constraints appear from foreknowledge about the shape of the optimum WF, the actual computation of $w(t)$ was never required for the optimization problem formulation. For illustration purposes, the length of the filter N was assumed to be an even number. Considering these constraints, minimizing the ENC^2 is equivalent to minimizing its numerator, and according to (3.14), the resulting objective function f_o is given by

$$\begin{aligned} f_o = \sum_{i=1}^{N} \Bigg\{ & \left(\sum_{h=0}^{N-i} a_{i+h} \sqrt{\sigma^2_{\text{shot}}((h+1)T_s) - \sigma^2_{\text{shot}}(hT_s)} \right)^2 \\ & + \left(\sum_{h=0}^{N-i} a_{i+h} \sqrt{\sigma^2_{\text{th}}((h+1)T_s) - \sigma^2_{\text{th}}(hT_s)} \right)^2 \\ & + \left(\sum_{h=0}^{N-i} a_{i+h} \sqrt{\sigma^2_{1/f}((h+1)T_s) - \sigma^2_{1/f}(hT_s)} \right)^2 \Bigg\}. \end{aligned} \tag{3.32}$$

To obtain a numerical solution for the optimization problem, given by the objective function (3.32) and constraints (3.30) and (3.31), the parameters of an HPGe segmented detector with an input FET transistor were considered. Assuming that the input device is in strong inversion, the coefficient a_T can be calculated as

$$a_T = \frac{2KT\gamma}{g_m} \tag{3.33}$$

where K is the Boltzmann constant, T is the absolute temperature, g_m is the transconductance of the input device and γ is a constant factor, typically $\approx 2/3$ (Van Der Ziel, 1970).

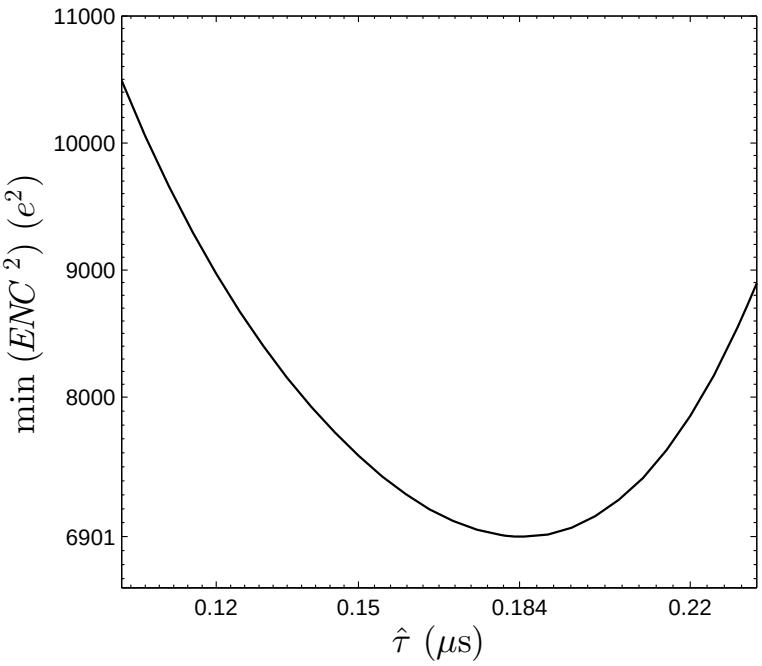

FIGURE 3.7. Minimum ENC^2 as a function of $\hat{\tau}$ for a fixed N.

The following parameters, typical of an HPGe segmented detector (Pullia & Riboldi, 2004), were used: $T = 120\,\mathrm{K}$, $g_m = 15\,\mathrm{mS}$, $R_F = 1\,\mathrm{G\Omega}$, $I_L = 100\,\mathrm{pA}$, $C_T = 40\,\mathrm{pF}$, $C_F = 1\,\mathrm{pF}$ and $a_F = 10^{-15}\,\mathrm{V}^2$. Additionally, the following parameters were arbitrarily selected: $t_m = 10\,\mu\mathrm{s}$, $T_s = 0.5\,\mu\mathrm{s}$ and $h_w = 1$.

The optimization problem was formulated in MATLAB and then solved through convex optimization with CPLEX (IBM, n.d.). Figure 3.7 shows the optimum value of the ENC^2 as a function of $\hat{\tau}$, where the existence of a global optimum at $\hat{\tau} = 0.184\,\mu\mathrm{s}$ can be seen. Figure 3.8 shows the optimum WF for different values of $\hat{\tau}$. Using the optimum WF and the noise parameters shown above the ENC can be computed as described in (Gatti & Manfredi, 1986) and (Pullia, 1998).

The initial assumption that the filter sampling period T_s is determined by the filter maximum clock rate is only valid if the optimum ENC^2 is lower bounded by T_s, or equivalently, by N. To support this assumption, Figure 3.9 shows the optimum value of the ENC^2 as a function of N. Although Figure 3.9 suggests to use the filter at the maximum

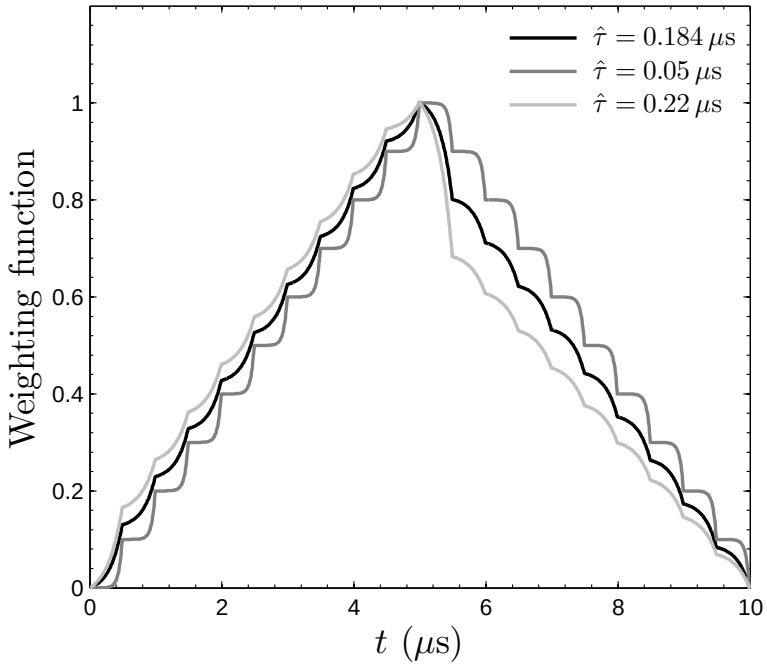

FIGURE 3.8. Optimum WF for different values of $\hat{\tau}$ for $N = 20$.

clock rate, for a large number of samples the contribution of an additional sample is marginal, thus to determine N other considerations should be taken into account, such as the filter power consumption and the filter design complexity. Additional requirements, such as flat-top or zero-area, can be easily added as constraints in the optimization problem.

3.5 Conclusion

This work presents a mathematical framework for the analysis of discrete-time filters in the discrete-time domain. The analysis is based on decomposing the total integrated noise at the filter input into a set of discrete-time noise signals, in order to refer them to the filter output and calculate the ENC. The proposed analysis only depends on the calculation of the total integrated noise at the filter input, which can be analyzed prior to taking into account the filter itself in order to understand and predict the noise behavior.

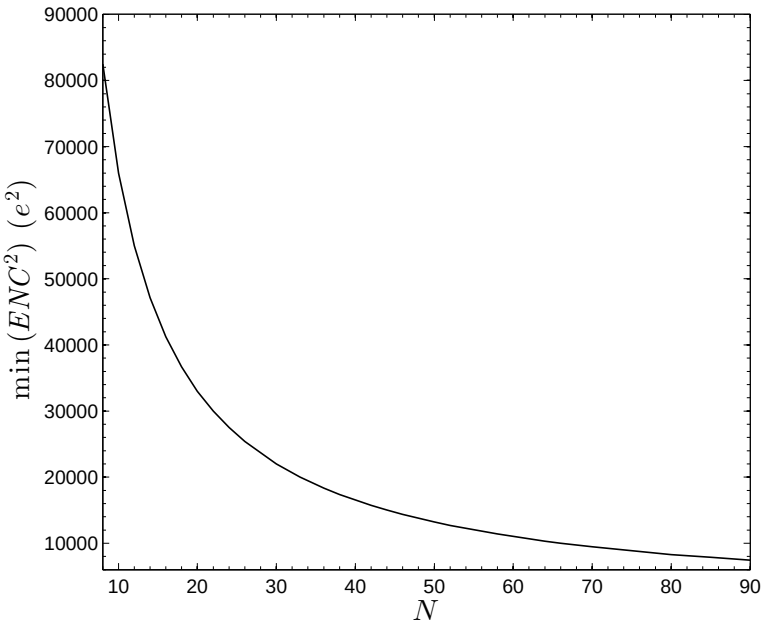

FIGURE 3.9. Optimum ENC^2 as a function of N for $\hat{\tau} = 0.03\,\mu$s.

In order to validate the proposed framework, the computation of the thermal noise contribution at the output of a discrete-time integrator is presented, and the result is compared to the result produced by the traditional continuous-time approach. Although both methods produce mathematically equivalent results, the former is simpler and more insightful.

This work also presents an example of optimal filter computation, in order to demonstrate the proposed framework capabilities and its application to optimization problems with several noise sources.

4. A SC FILTER FOR ARBITRARY WEIGHTING FUNCTION SYNTHESIS

4.1 Introduction

One of the greatest benefits of the mathematical framework presented in (Avila et al., 2013) is that it allows to easily find the optimal discrete-time filter that minimizes the noise of a typical detector front-end circuit, a difficult task to undertake using the traditional methods for continuous-time networks. The filter presented in this chapter is designed to be flexible enough to synthesize arbitrary weighting functions with an adequate resolution. Therefore, it could be used to synthesize the optimal filter described above. The filter is a prototype of the front-end filter for the Bean V2, which was introduced in Chapter 2. Hence, the main specifications are derived from the Bean specifications. Also, power, noise and size budgets of the referred IC are taken as constraints.

There are two common options for implementing the required filter. The simplest is to digitize the CSA output directly with a fast analog-to-digital converter (ADC) - N times faster than the typical used ADC, with N the number of desired samples - and then process the samples in the digital domain, whereas the other option is to use a custom switched-capacitor (SC) network as a filter, without changing the ADC requirements. Considering the Bean timing constraints, the former option is not feasible, given that such fast ADC would exceed the available power and size budgets. Hence, the SC solution was finally chosen.

4.2 System-Level Design

As mentioned in the previous Chapter, to synthesize arbitrary weighting functions the front-end filter should be designed to have a discrete-time transfer function $F(z)$ given by

$$F(z) = \sum_{j=0}^{N-1} a_{N-j}\, z^{-j} \tag{4.1}$$

where a_i are the filter gain coefficients and N is the filter length. Fig. 4.1 shows a simplified circuit diagram of a fully-differential SC integrator designed to implement $F(z)$. Some control logic and switches have been purposely omitted.

The filter has two phases of operation. During the sampling phase, ϕ_1, the input voltage charges both C_S capacitors. During the amplification phase, ϕ_2, the OTA input virtual short circuit forces charge from capacitors C_S to be transferred to capacitors C_F. Thus, at the end of ϕ_2, the filter output voltage is equal to its value in the previous cycle, plus $C_S V_i / C_F$. Also, an early version of ϕ_1, ϕ_{1e}, is used in the sampling phase to implement Bottom-Plate Sampling (Haigh & Singh, 1983), a technique used to reduce the charge injection from switches.

In this configuration, the filter instantaneous gain is given by the ratio of the capacitors C_S and C_F. Considering that in order to obtain arbitrary coefficients the filter gain must be programmable, either C_S or C_F should be implemented with a variable capacitor. For simplicity, capacitor C_S was selected for this purpose. The OTA input multiplexers are used to swap the OTA inputs, and therefore, to invert the sign of the filter gain. The OTA output common-mode level is set by the OTA's internal common-mode feedback (CMFB) circuit, whereas the input common-mode level is set by the external reference V_{icm}. The OTA output multiplexers are used to bypass the filter for the SDT operation mode and for diagnostic purposes.

4.2.1 Filter Specifications

Table 4.1 summarizes the filter specifications derived from the Bean specifications (Table 2.1). Also, the CSA output specifications and the ADC input specifications were taken into account. The sampling frequency is $51.95\,$MHz. Thus, each integration subcycle is $19.25\,$ns long. Since each subcycle involves two phases, sampling and holding, each phase has only $9.625\,$ns for settling. Considering this time, to assure a dynamic error of $0.1\,\%$ (to meet the dynamic range specification) the amplifier must have a worst-case closed-loop bandwidth of $f_u = 118\,$MHz (without considering slew-rate regime). Also, a static error of $0.1\,\%$ is required, which implies an OTA open-loop gain of at least $60\,$dB.

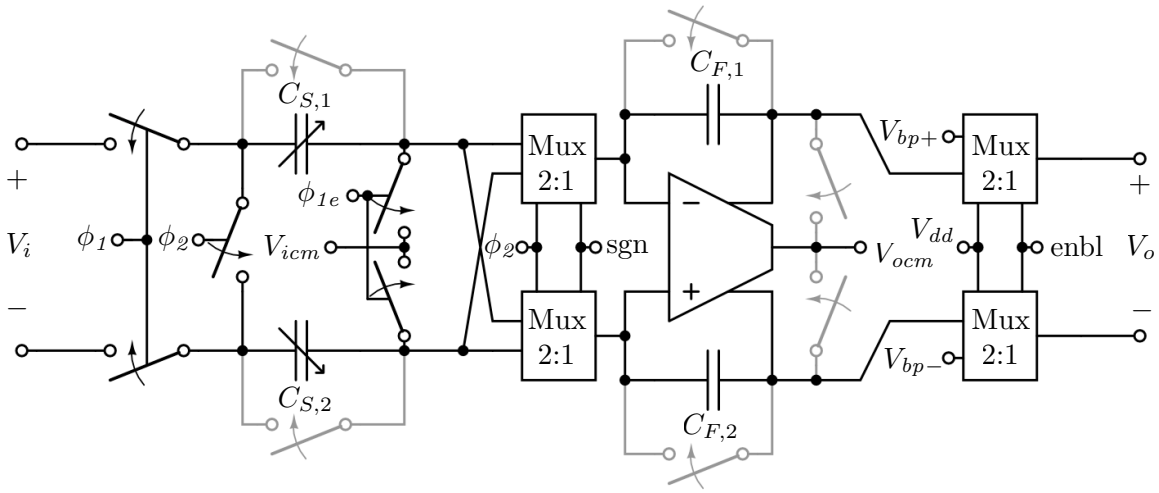

FIGURE 4.1. Simplified filter schematic. Reset switches are depicted in gray.

Specification	**Value**
Modes of operation	SDT and DCal
Input swing	0.9 V or close
Output swing	1 V or close
Dynamic range	10 bits
Gain resolution	6 bits (7.8 mV/V - 0.5 V/V)
Noise budget	$1.25 \times Q_n^2$
Operation speed	51.95 MHz
Power consumption	Minimize

TABLE 4.1. Filter specifications summary, where Q_n^2 is the readout ADC quantization noise.

4.3 Circuit Design

4.3.1 Operational Transconductance Amplifier

The previous version of the Bean uses a two-stage Miller-compensated OTA as the filter amplifier. However, this topology does not lead to a feasible design given the filter specifications, mainly, because of the existing trade-off between noise and bandwidth, resulting from the Miller capacitor. For this version of the Bean, a single-stage OTA

topology was chosen, as it can theoretically meet the filter specifications. A folded cascode (FC) OTA would be the first candidate to implement this amplifier, because of its good balance between gain, speed, input-output swing and complexity. Nonetheless, the settling-time specification would require high bias currents due to the slew-rate limitation, which would come into conflict with the power budget. The recycling folded cascode OTA (RFC) (Assaad & Silva-Martinez, 2009), a small variation over the FC OTA, was chosen to overcome this limitation, since it exhibits an enhanced transconductance, gain, and slew-rate (SR) over the conventional FC OTA for the same power and size budgets.

In a traditional FC OTA, folding transistors conduct most of the current and generally have the largest transconductance. However, their role is only limited to providing a folding node for the small signal current (Assaad & Silva-Martinez, 2009). In a RFC OTA (Fig. 4.2), a small modification over the conventional FC topology allows to use the folding transistors as additional drivers for the small signal input. Therefore, they are used to enhance the effective transconductance of the amplifier. Also, this modification entails additional enhancements over the conventional FC OTA, such as higher and symmetrical SR, higher output resistance and higher crossover-frequency.

In a voltage-controlled voltage source (VCVS), such as the filter amplifier, the low-frequency open-loop gain can be calculated as $|A_V| = G_{m,eff} \cdot R_o$, where $G_{m,eff}$ is the effective transconductance, defined as the ratio of the incremental short-circuit output current to the input voltage, and R_o is the output resistance, defined as the resistance seen at the amplifier output when no input is applied (Rashid, 2010). In a RFC OTA the effective transconductance can be approximated to:

$$G_{m,eff} \approx g_{m,in}(1 + K) \tag{4.2}$$

where K is the current mirror ratio between transistors M_f and $M_{aux,3}$. Also, the output resistance can be approximated to:

$$R_o \approx g_{m,cf} r_{o,cf} \left((r_{o,in} \parallel r_{o,aux3}) \parallel (g_{m,cl} r_{o,cl} r_{o,l}) \right) \tag{4.3}$$

Considering that the RFC OTA is a single-stage amplifier, and assuming a proper design, the dynamic behavior of the open-loop filter will be dominated by the output node resistance and the load capacitance, C_L, so other time constants can be ignored. For a RFC OTA, the unity-gain bandwidth, ω_u, is given by:

$$\omega_u = \frac{G_{m,eff}}{C_L} \tag{4.4}$$

Once integrated in the filter, all non-dominant poles and zeros will be beyond the unity-gain frequency. Thus, the closed-loop bandwidth, ω_c, can be approximated to:

$$\omega_c = \beta \frac{G_{m,eff}}{C_{L,tot}} \tag{4.5}$$

where β is the feedback factor, given by

$$\beta \approx \frac{C_F}{C_F + C_S + C_{\text{parasitic}}} \tag{4.6}$$

and $C_{L,tot}$ is the total load capacitance, given by:

$$C_{L,tot} = C_L + (1 - \beta)C_F \tag{4.7}$$

where $C_{\text{parasitic}}$ is the parasitic capacitance at the OTA input node.

In a RFC OTA the SR is symmetrical and enhanced K times over the FC OTA for the same power consumption. Considering I_{tail} as the bias current of the transistor M_{tail}, the SR can be computed as:

$$\text{SR} = \frac{2KI_{tail}}{C_L} \tag{4.8}$$

In a SC integrator, noise is sampled at both clock phases, namely ϕ_1 and ϕ_2. Thus, to calculate the filter output-referred total integrated noise, both noise contributions must be calculated separately and added up in quadrature. After N integration cycles and assuming an arbitrary C_S at each cycle, the contribution from noise sampled at ϕ_1 can be computed as:

$$\overline{V_{\phi_1}^2} = 2kT \sum_{i=1}^{N} \frac{1}{C_F} \left(1 + \frac{C_{S_i}}{C_F}\right) \tag{4.9}$$

Transistor	Bias current	g_m/I_D	W	L
M_{in}	$51.3\,\mu\text{A}$	$14.9\,\text{mS/mA}$	$48\,\mu\text{m}$	$0.36\,\mu\text{m}$
M_{tail}	$201.7\,\mu\text{A}$	$8.2\,\text{mS/mA}$	$64\,\mu\text{m}$	$0.45\,\mu\text{m}$
M_{f}	$100.6\,\mu\text{A}$	$8.7\,\text{mS/mA}$	$8\,\mu\text{m}$	$0.45\,\mu\text{m}$
M_{cf}	$49.3\,\mu\text{A}$	$11.7\,\text{mS/mA}$	$8\,\mu\text{m}$	$0.45\,\mu\text{m}$
M_{cl}	$49.3\,\mu\text{A}$	$10.7\,\text{mS/mA}$	$16\,\mu\text{m}$	$0.3\,\mu\text{m}$
M_{l}	$49.3\,\mu\text{A}$	$7.6\,\text{mS/mA}$	$32\,\mu\text{m}$	$1\,\mu\text{m}$
$M_{\text{aux,1}}$	$49.6\,\mu\text{A}$	$15\,\text{mS/mA}$	$48\,\mu\text{m}$	$0.36\,\mu\text{m}$
$M_{\text{aux,2}}$	$49.6\,\mu\text{A}$	$9.5\,\text{mS/mA}$	$2\,\mu\text{m}$	$0.18\,\mu\text{m}$
$M_{\text{aux,3}}$	$49.6\,\mu\text{A}$	$6\,\text{mS/mA}$	$4\,\mu\text{m}$	$0.45\,\mu\text{m}$

TABLE 4.2. Filter OTA design values.

In a proper design, switch resistances will be much smaller than $1/(\beta g_{m,eff})$, so noise at ϕ_2 can be assumed to be dominated by the OTA noise (Vleugels, 2011). Thus, the noise contribution at ϕ_2 can be approximated to:

$$\overline{V_{\phi_2}^2} \approx \frac{2N_f kT\gamma}{g_{m,eff}} \sum_{i=1}^{N} \frac{1}{\beta_i C_{Ltot_i}} \tag{4.10}$$

where N_f is a noise factor dependent on the single-stage OTA topology, for a RFC:

$$N_f \approx \frac{1}{1+K}\left(\frac{1+K^2}{1+K} + \frac{g_{m,f}}{g_{m,in}} + \frac{1}{1+K}\frac{g_{m,l}}{g_{m,in}}\right) \tag{4.11}$$

Table 4.2 shows the parameter values for the OTA design. Transistor sizes were calculated using equations 4.2 to 4.11 and a semi-exhaustive search script, with tabulated pre-simulated data and using the g_m/I_D design technique (Silveira, Flandre, & Jespers, 1996). Computational power was not a problem at this point. However, for a deeper optimal design, a bigger domain must be chosen (not increasing the boundaries but increasing the domain resolution) and an intelligent algorithm must be used, e.g like the use of Support Vector Machines in (Bernardinis, Jordan, & Sangiovanni-Vincentelli, 2003) to reduce the feasible domain of solutions. SPICE simulations predict an open-loop DC gain of $72\,\text{dB}$, a crossover frequency of $150\,\text{MHz}$, and a phase margin of 75° measured with an $0.4\,\text{pF}$ load.

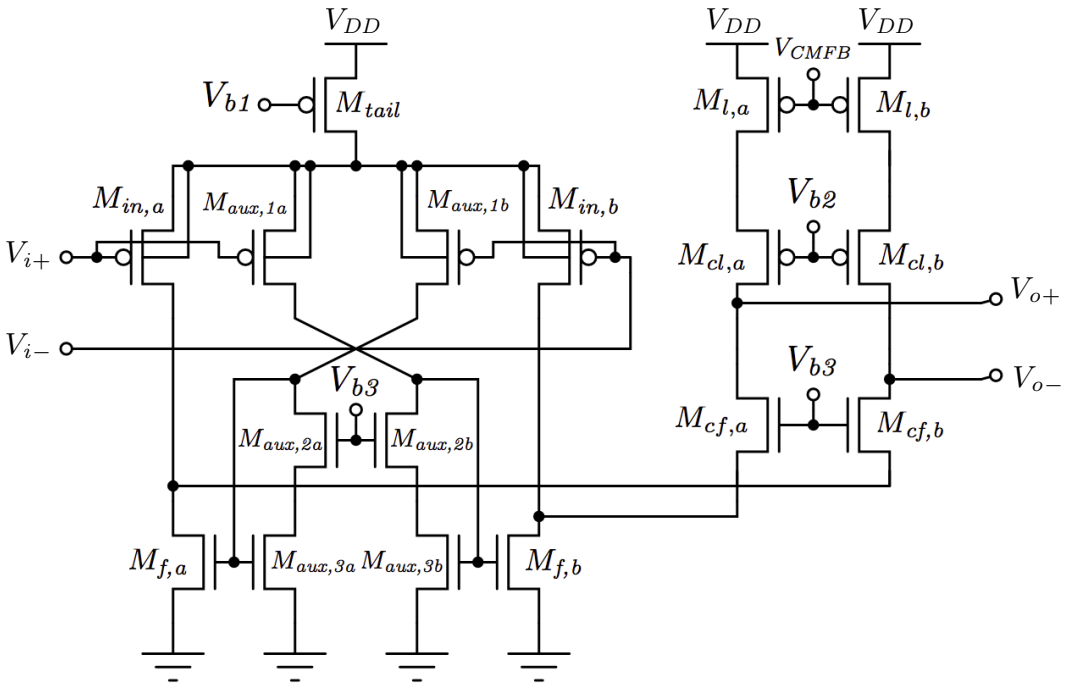

FIGURE 4.2. Recycling folded cascode OTA schematic. Three terminal NMOS and PMOS devices are with their bodies tied to ground and V_{DD} respectively. CMFB circuit is shown in Fig. 4.3

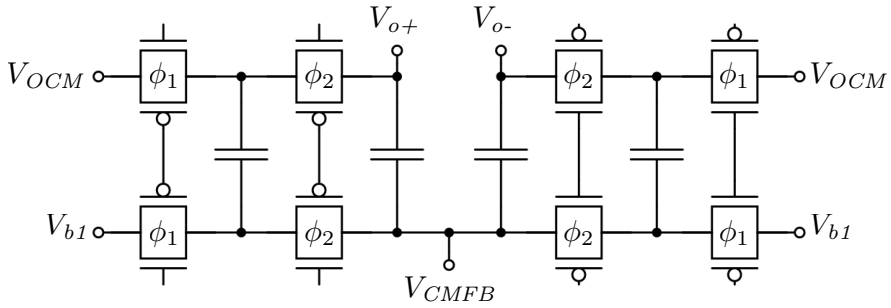

FIGURE 4.3. OTA discrete-time commmon-mode feedback circuit schematic.

4.3.2 Variable Capacitor

Fig. 4.5 shows the schematic of the binary-weighted array used to implement the variable capacitor C_S. All capacitors $C_{S,bn}$ were designed as a parallel connection of unity metal-insulator-metal (MIM) capacitors $C_u = 8.1\,\text{fF}$ (with an area of $2.7\,\mu\text{m} \times 2.7\,\mu\text{m}$), which for matching purposes were also used to implement capacitor C_F. CMOS switches

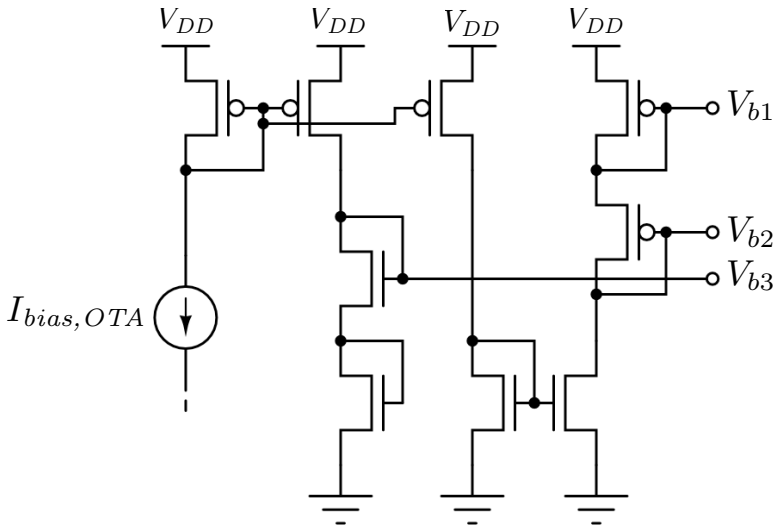

FIGURE 4.4. OTA bias network schematic.

were sized to meet filter speed specifications. Switch control signals will be directly bonded out off-chip. A serial-programmable memory to store the filter coefficients, and which will be connected directly to these control signals - to avoid the unnecessary use of IC pads -, will be included in future revisions of the Bean.

4.3.3 Rail-to-Rail buffer

A signal buffer is required to buffer some of the Bean prototype voltages for scope probing. The buffer must be able to drive a $8\,\mathrm{pF}$ load at a reasonable speed and power dissipation, with truly rail-to-rail input and output voltages. Fig. 4.6 shows the schematic of a rail-to-rail operational amplifier (op-amp) used to implement a unity-gain voltage buffer amplifier.

The two-stage op-amp consists of a rail-to-rail constant-g_m input stage (Hogervorst, Tero, & Huijsing, 1995), composed by two complementary input pairs and an electronic zener diode, M_{in1}-M_{in2}, $M_{\mathrm{ip,a}}$-$M_{\mathrm{ip,b}}$ and M_{zp}-M_{zn}, followed by folded-cascode, current-mirroring loads, M_{cln1}-M_{ln1}, M_{cln2}-M_{ln2}, M_{clp1}-M_{lp1} and M_{clp2}-M_{lp2}, and a class-AB output (Hogervorst, Tero, Eschauzier, & Huijsing, 1994), M_{op}-M_{on}. Transistors M_{sn1}-M_{sn2} and M_{sp1}-M_{sp2} implement a translinear loop (Sansen, 2006), producing the voltage shifts necessary to set the output devices quiescent current consumption.

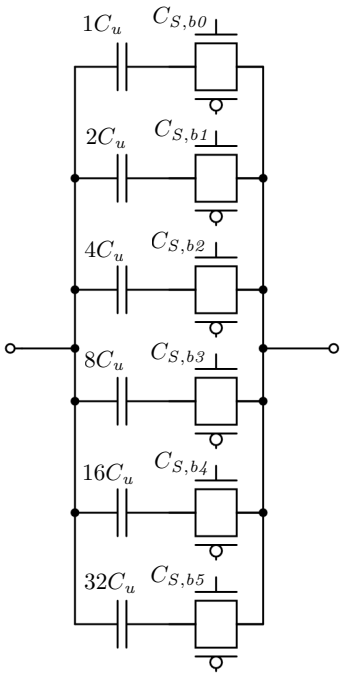

FIGURE 4.5. 6-bit programmable capacitor.

As in most of two-stage amplifiers, stability must be assured with a proper compensation scheme. In this design, capacitor C_C, also known as Miller capacitor, is placed to lower the frequency of the dominant pole and to increase the frequency of the secondary pole, and thus, it helps to increase the phase margin of the amplifier, while resistor R_Z is used to shift to infinity the right-half plane zero that appears because adding C_C. Since C_C is calculated as a function of the input stage's total transconductance, the constant-g_m compensation technique used for the input stage helps to maintain a constant frequency response over all the input common mode range.

To assure predictable bias currents and a true rail-to-rail input and output voltage ranges, a proper bias network must be designed. Fig. 4.7 shows the schematic of the bias network used for this op-amp (Baker, 2010). All bias voltages are driven by cascoded current mirrors, which have high output resistance in order to reduce the effect of V_{ds} over

Transistor	Bias current	g_m/I_D	W	L
M_{in}	$10.4\,\mu$A	$21.2\,$mS/mA	$12.8\,\mu$m	$0.45\,\mu$m
M_{ip}	$9.2\,\mu$A	$19.4\,$mS/mA	$40\,\mu$m	$0.45\,\mu$m
M_{tp}	$60.6\,\mu$A	$7.4\,$mS/mA	$20\,\mu$m	$0.45\,\mu$m
M_{tn}	$62.9\,\mu$A	$9.2\,$mS/mA	$6.4\,\mu$m	$0.45\,\mu$m
M_{lp}	$26.3\,\mu$A	$9.1\,$mS/mA	$10\,\mu$m	$0.45\,\mu$m
M_{clp}	$16\,\mu$A	$14.2\,$mS/mA	$20\,\mu$m	$0.45\,\mu$m
M_{ln}	$25.2\,\mu$A	$10.9\,$mS/mA	$3.2\,\mu$m	$0.45\,\mu$m
M_{cln}	$16\,\mu$A	$16.8\,$mS/mA	$6.4\,\mu$m	$0.45\,\mu$m
M_{op}	$282\,\mu$A	$9\,$mS/mA	$100\,\mu$m	$0.45\,\mu$m
M_{on}	$282\,\mu$A	$10.7\,$mS/mA	$32\,\mu$m	$0.45\,\mu$m

TABLE 4.3. Rail-to-rail buffer main design values.

the mirrored current. Transistor sizes were calculated to assure a maximum amplifier output swing and mirror currents were chosen to maintain a good tradeoff between mirrored currents sensibility and bias network power consumption.

Table 4.3 shows the parameter values for the rail-to-rail buffer design. Transistor sizes were calculated with the same methodology as that used for the OTA design. SPICE simulations predict an open-loop DC gain of $103\,$dB, a crossover frequency of 52,MHz, and a phase margin of 72° measured with an $8\,$pF load.

4.3.4 IC bias network

The previous version of the Bean uses a voltage distribution scheme to bias all the circuits in the IC, but it can cause big problems due to IR drop and process gradients, so a more common current distribution scheme was chosen for this iteration of the design (Murmann, 2007). The main disadvantage of this architecture is the additional current consumption, but this drawback is marginal compared to the entire IC power budget and the obtained benefits. To achieve a good power supply rejection (PSR), a supply-insensitive bias network was chosen to implement the global bias cell, from which all the bias currents are generated. Fig. 4.8 shows a diagram of the current distribution bias scheme. For simplicity, only three current branches are illustrated, although five were used in the final design. Fig. 4.9 shows the schematic of a β-multiplier bias circuit, the

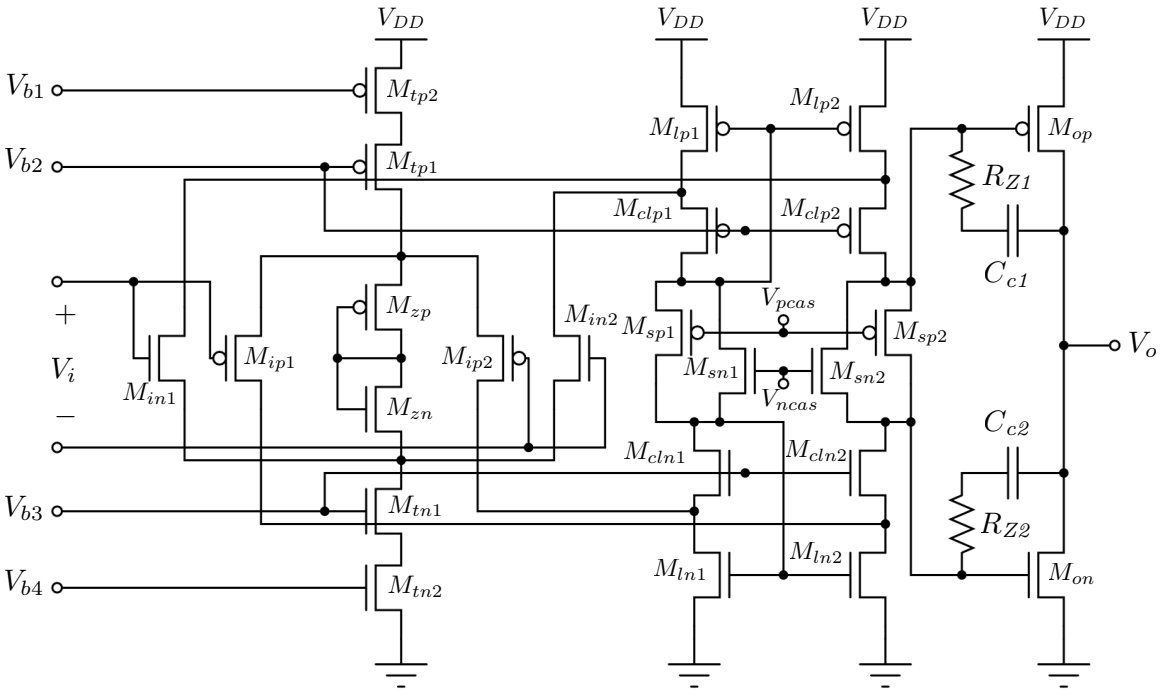

FIGURE 4.6. Rail-to-rail operational amplifier schematic.

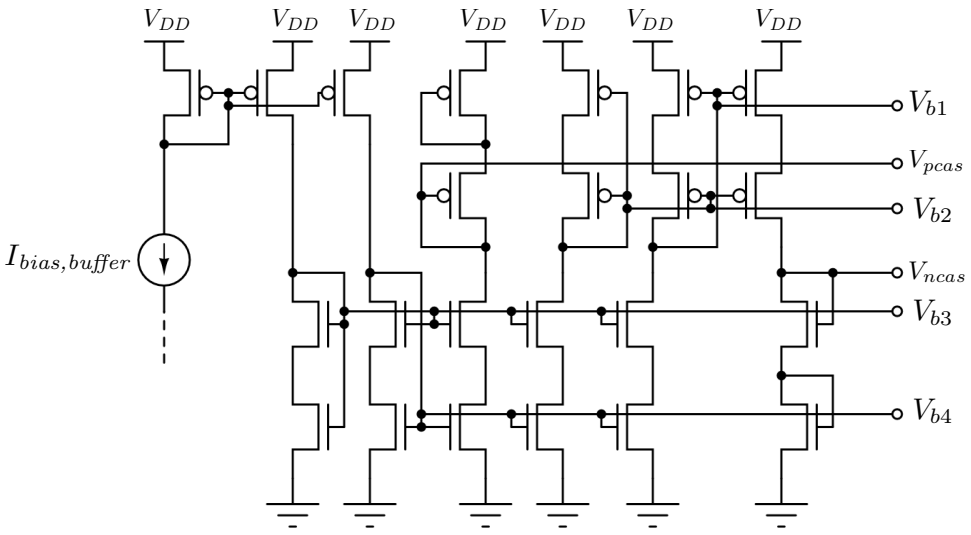

FIGURE 4.7. Op-amp bias network schematic.

architecture selected to implement the supply-insensitive bias network. This consist of a self-biased current-reference network, a start-up circuit, because there are two possible operating points, and a cascode current mirror. The β-multiplier is an example of a circuit

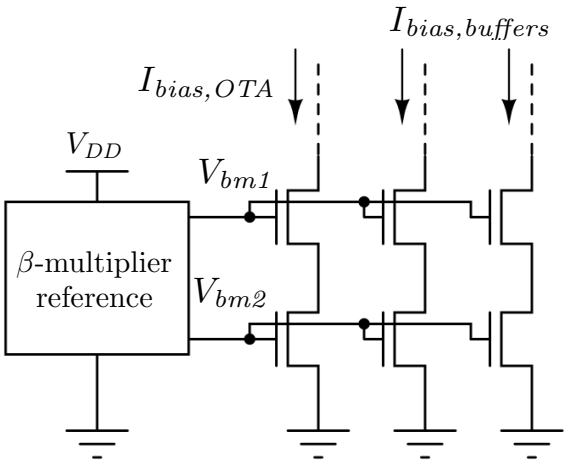

FIGURE 4.8. Current distribution bias scheme.

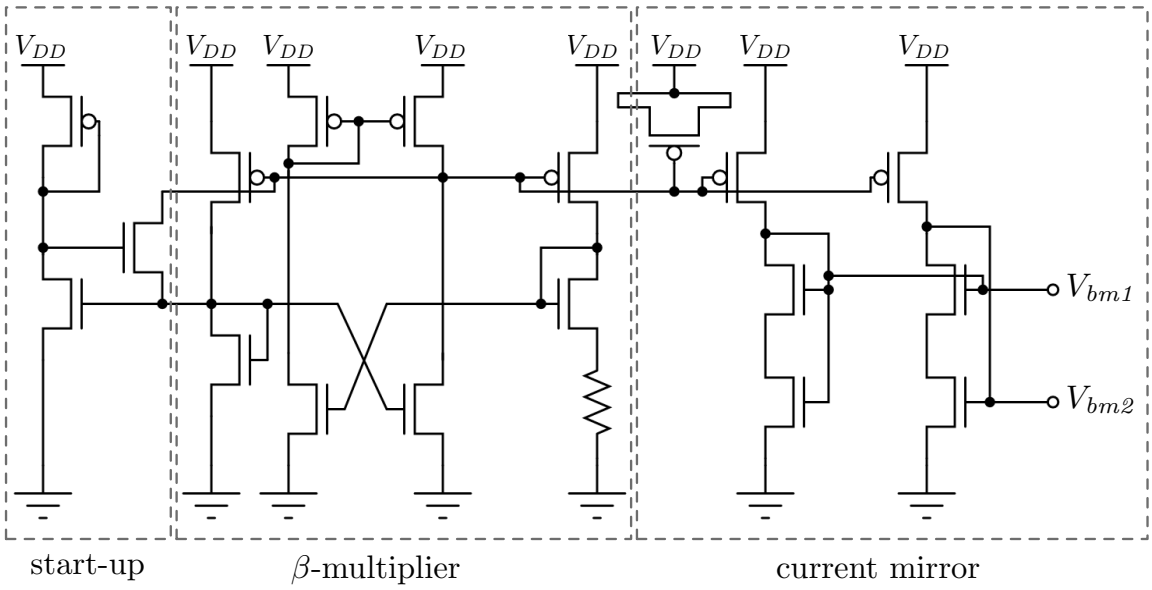

FIGURE 4.9. β-multiplier bias schematic.

that uses positive feedback. The addition of the resistor kills the closed loop gain[1]. However, if the parasitic capacitance of this resistor is large, it will increase the loop gain and push the feedback system closer to instability. If the resistor, for example, is bonded out off-chip to set the current, it is likely that this bias circuit will oscillate (Baker, 2010).

[1] A positive feedback system can be stable if its closed loop gain is less than one.

5. RESULTS

5.1 The Bean V2 prototype Implementation

The Bean V2 prototype was designed for a standard mixed-signal 180-nm CMOS process. This iteration of the Bean includes two standalone structures: a trimmed version a readout channel, which includes two CSA (one with its input and output connected, to generate the baseline voltage[1]), a pre-charger circuit, the designed SC filter and output buffers; and an isolated version of the filter with its inputs directly bonded out off-chip. Both structures will be tested separately, thus control signals and reference voltages for both filters are tied together. Also, a logic circuit to generate the non-overlapping two-phase clock was included. Future revisions of the prototype will include a 10-bit SAR ADC and a digital memory within the channel.

Fig. 5.1 shows the layout of the Bean V2 prototype; for a detailed description of the IC pinout, see Appendix A. Each channel cell was designed to have a pitch lower than $190\,\mu$m. If the number of channels is increased to the nominal value of 32, the IC will be approximately 6 mm tall, which can be fit into four mini@sic sub-blocks according to the Europractice rules. After including the ADC and the digital memory, channel length is expected to be lower than 1 mm.

The SC filter, shown in Fig. 5.2, has a total area of $185\,\mu\text{m} \times 332\,\mu\text{m}$, and was laid out to resemble the components spatial distribution of the circuit in Fig. 4.1. The filters outputs, the main CSA output and the baseline voltage are buffered out off-chip using the rail-to-rail amplifiers (connected as unity-gain buffers) shown in Fig. 5.5. The CSA and the filter OTA are depicted in Figs. 5.3 and 5.4 respectively. All structures were carefully side-shielded with multiple guard-rings. Also, to mitigate the effects of cross-chip gradients, the common-centroid technique and dummy devices were used in the layout of the filter OTA and the rail-to-rail op-amps. These considerations were not taken into account for the

[1]The baseline is defined as the CSA DC output voltage after reset, when no input has been applied.

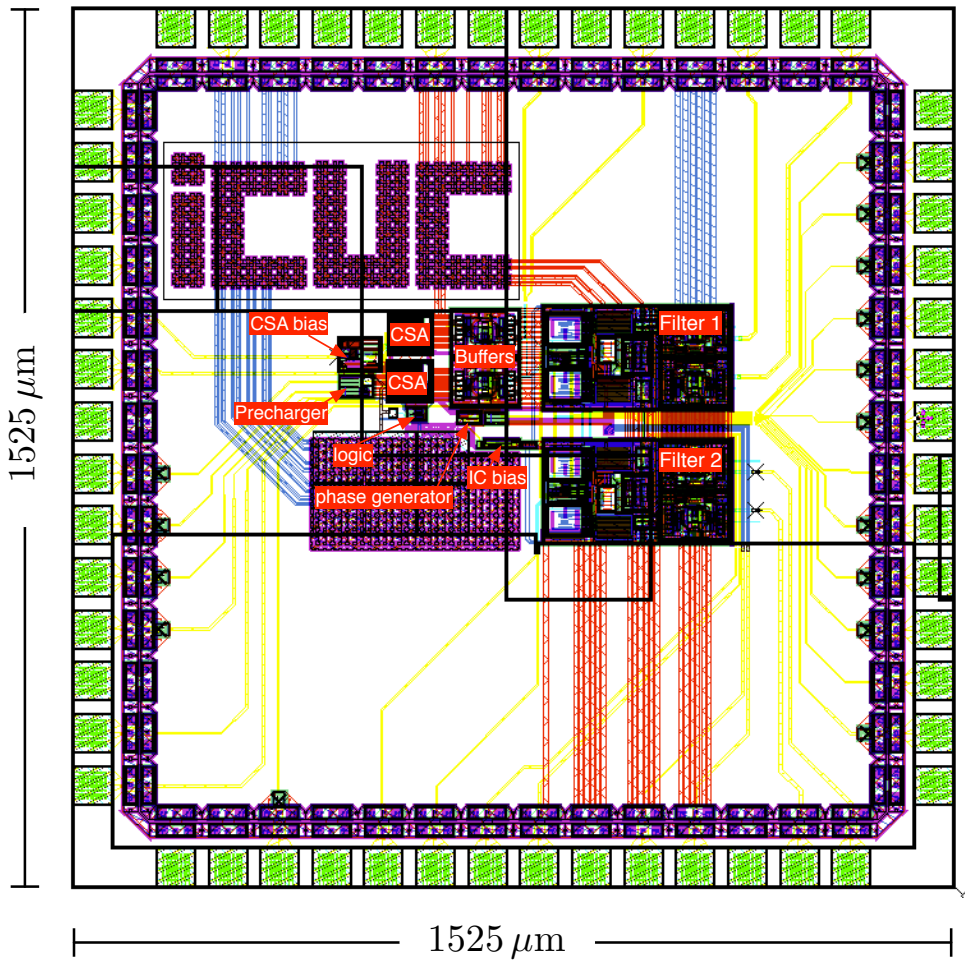

FIGURE 5.1. The Bean V2 prototype layout.

CSA layout, since mismatch is not critical for this cell because of the size of its transistors and because it is a single-ended device. As mentioned in the previous chapter, capacitors C_F and C_S were implemented with a parallel connection of unity MIM capacitors. To prevent copper-dishing effects, both capacitors were surrounded by dummy capacitors implemented with the same unity capacitors.

Because of the lack of models for the pads provided by Faraday and the tools needed to use them, it was necessary to design custom pads. They were designed for ground, positive supply voltage, analog input/output, digital input, and digital output. Special

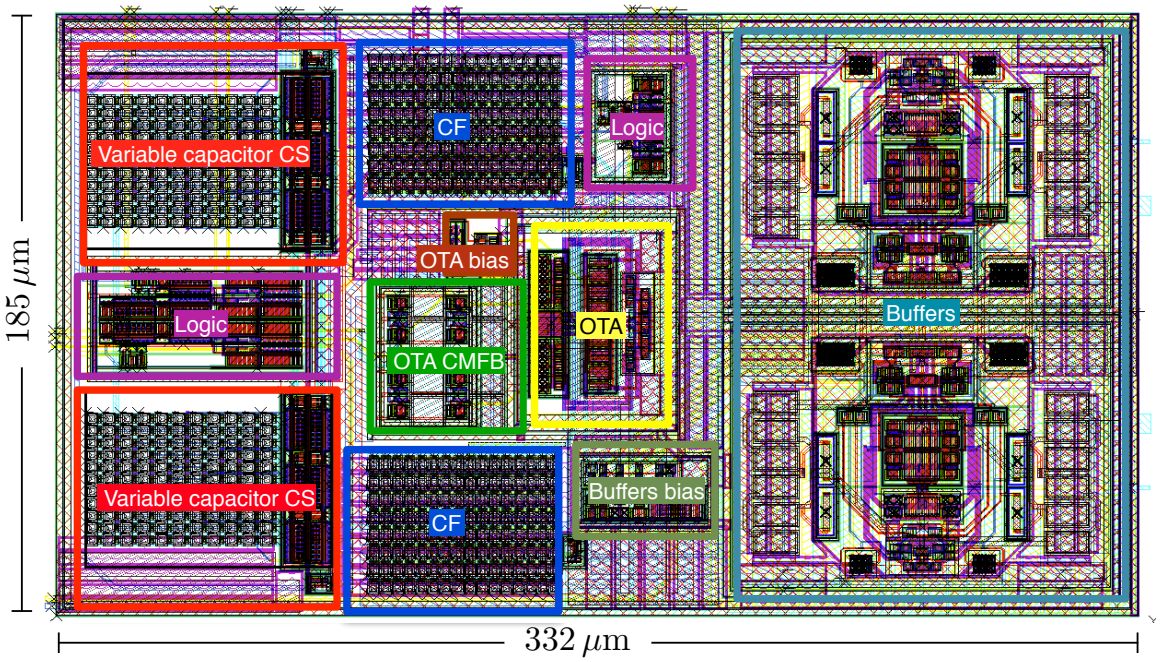

FIGURE 5.2. Filter Layout.

care was taken for the Latch-up failure of the output digital drivers, and the electrostatic discharge phenomena.

5.2 Filter post-layout simulation results

5.2.1 Sub-blocks

The filter OTA and the buffer op-amp are the complex sub-blocks of the design. Thus, before proceeding with the complete layout, both structures were extracted separately and simulated individually. Figs. 5.6 and 5.7 shows the simulated open-loop response of the filter OTA and the buffer op-amp, respectively. The results are very close to the pre-layout simulation results of Chapter 4, the most important difference is that the phase margin of the op-amp is 8° lower than the pre-layout estimation. However, it is still within a safe and stable margin. To prove stability, exhaustive transients simulations were run using sharp voltage steps on the inputs, the power supply and the different voltage references. Special care was taken to prove stability of the β multiplier circuit.

Component	Current dissipation
Filter OTA	$369\,\mu$A
Filter bias and logic	$194\,\mu$A
Unity-gain buffer	$360\,\mu$A

TABLE 5.1. SC filter simulated current dissipation.

5.2.2 Power dissipation

The power dissipated by the SC filter prototype was estimated using transient simulations over the extracted filter, under nominal operation and a single input value. The results are presented in Table 5.1. The measurements are current consumption averages of the supply node of each component, thus, taking into account dynamic power consumption of the logic circuits.

5.2.3 Functionality

A transient simulation using the entire extracted SC filter, including the bias structures, the buffers and the non-overlapping two-phase clock generator, was used to test the filter functionality. Control signals were driven with piecewise-linear voltage sources and a differential voltage step was used as filter input. Fig. 5.8 shows the simulation result. The measured waveform confirms the functionality of all blocks.

A single clock cycle transient simulation was used to test the variable gain functionality of the filter. The control signals for the variable capacitors were driven with piecewise-linear voltage sources and a differential voltage step was used as filter input. Fig. 5.9 shows the filter step response for the 64 available filter gains. The simulation confirms the monotonically increasing characteristic of the filter gain. However, the increments are not constant between consecutive filter gains. This can be explained due to the use of a binary array to implement the variable capacitor. This could be improved using a thermometer array or a mix between both, at the cost of adding complexity.

5.2.4 Linearity

The filter Integral nonlinearity (INL) was simulated for an input ramp covering 100% of the filter input range. The simulations were carried out for nominal speed, with an input ramp driven by an ideal voltage source. Fig. 5.10 shows the simulation result. The INL plot shows a typical second order non-linear behavior caused by variations over the filter OTA gain due to the input range. This can be improved with a constant-g_m OTA input stage and by increasing the OTA open-loop gain. Spikes on the INL plot are caused by simulation numerical errors, thus they do not represent any filter dysfunction. The high value of the INL is due to the insufficient time for the filter to settle. Future revision of the Bean should consider the filter dynamical behavior and take special attention to the common-mode feedback loop, which was one of the factors that affected the filter settling time in this iteration of the design.

5.2.5 Weighting function

The filter weighting function (WF) was simulated according to its definition described in Chapter 3. This was done by applying an input voltage step at different times within a cycle, and measuring the output at the measurement time. A simple RC network was used to simulate a voltage step as seen at the output of a CSA. Fig. 5.11 shows the circuit used to perform this measurement.

Fig. 5.12 shows the post-layout SPICE-simulated WF of the filter using flat coefficients and the Bean nominal clock frequency. As expected, its shape resembles the shape of the WFs in Fig. 3.8, which confirm the functionality of the filter to synthesize practical WFs. The initial non-zero value is caused by the successive integration of the filter input-referred offset voltage and the filter nonlinearities. Future revision of the filter could include a chopper-stabilized OTA to reduce the offset, and thus, to reduce the WF nonideality.

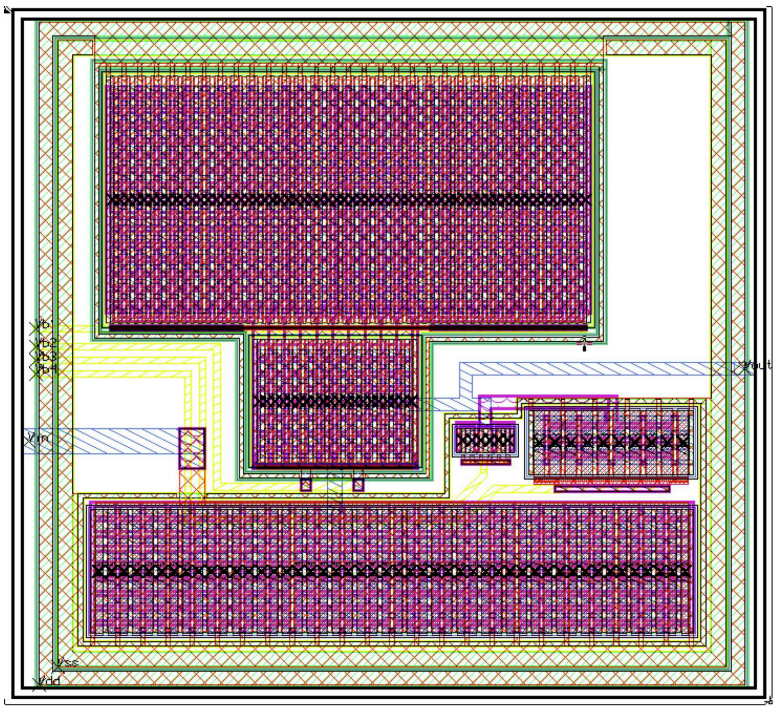

FIGURE 5.3. Charge-sensitive amplifier layout. Feedback capacitors are not included here.

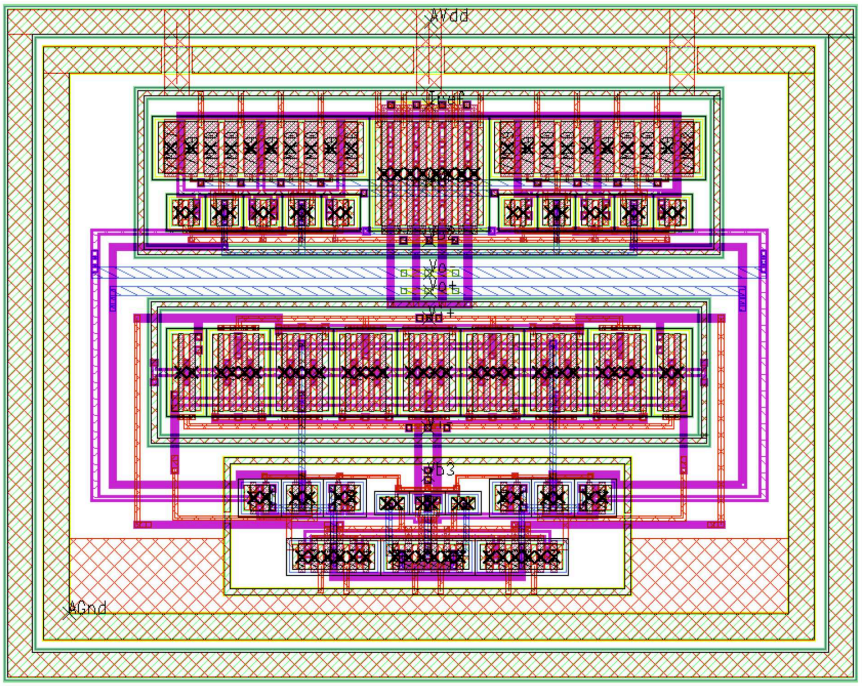

FIGURE 5.4. Recycling folded cascode OTA layout.

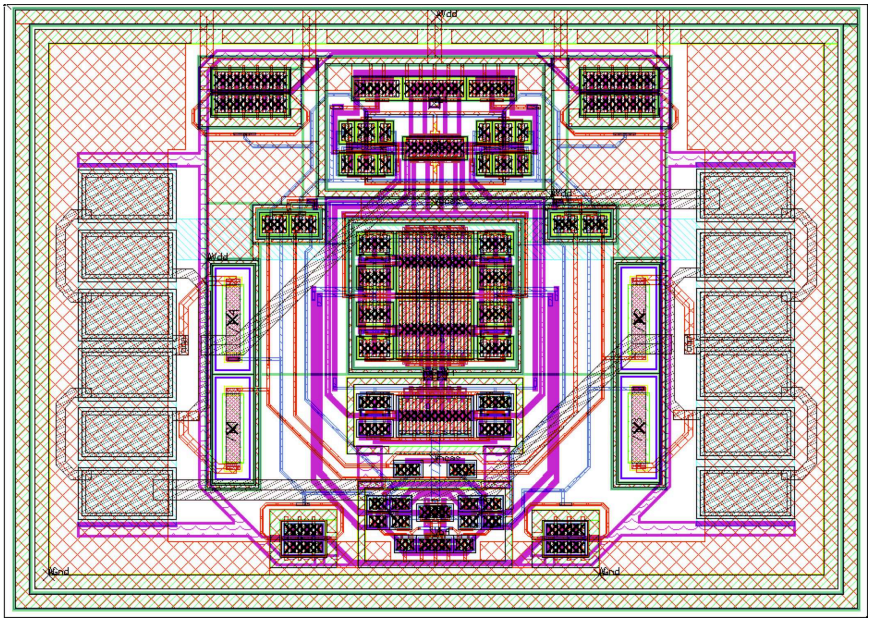

FIGURE 5.5. Rail-to-rail operational amplifier layout.

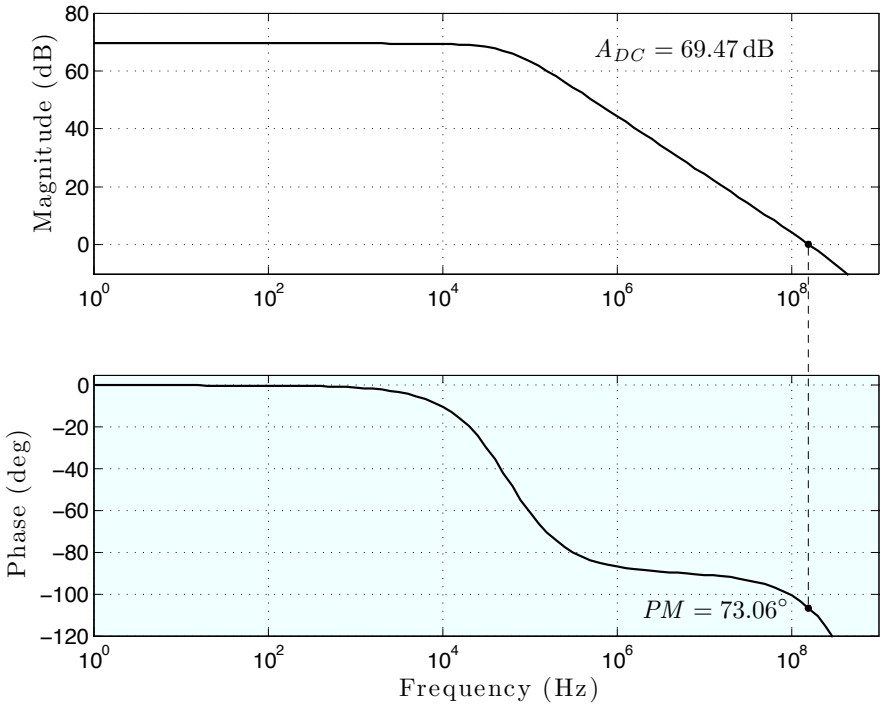

FIGURE 5.6. Bode plot for the OTA open-loop response, with a $0.4\,\mathrm{pF}$ load capacitance.

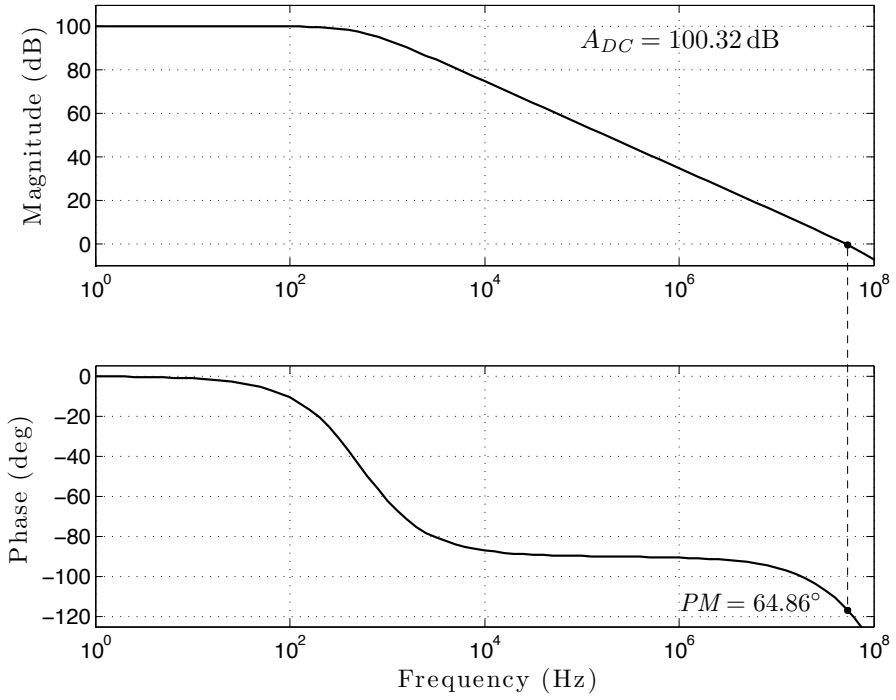

FIGURE 5.7. Bode plot for the buffer open-loop response, with a 8 pF load capacitance.

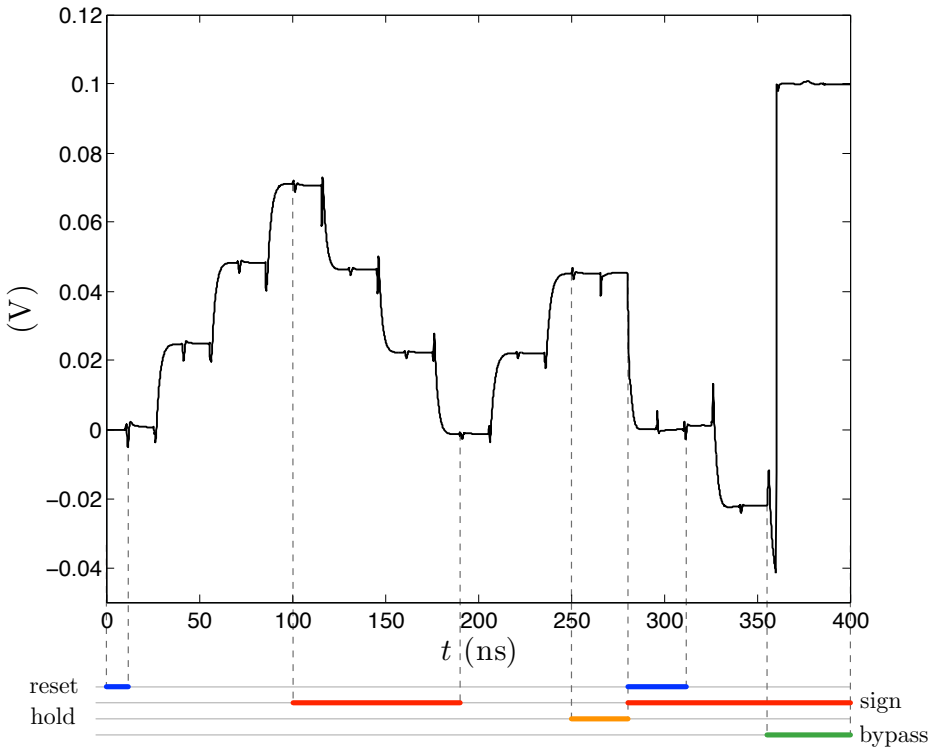

FIGURE 5.8. Filter functionality simulation. $V_{in} = 0.1\,V$ and gain $= 0.25\,V/V$.

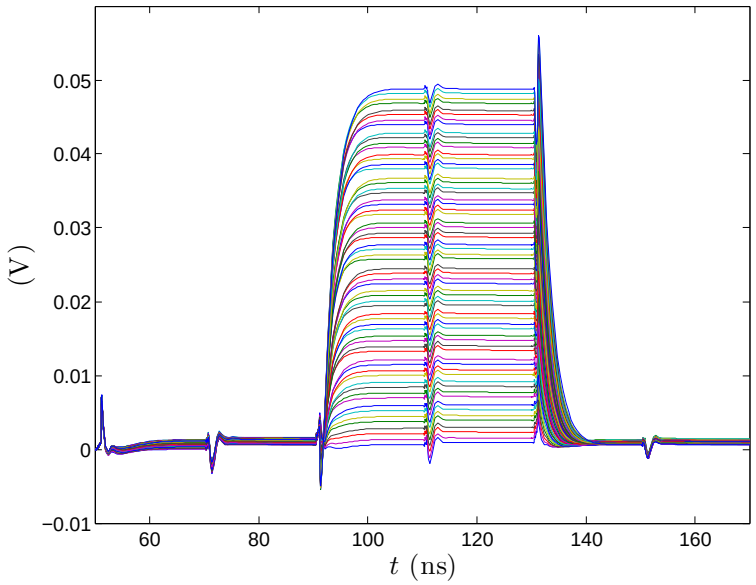

FIGURE 5.9. Filter step response for constant input for the 64 possible programmable gains. $V_{in} = 0.1\,V$ and $T_s = 40\,\text{ns}$.

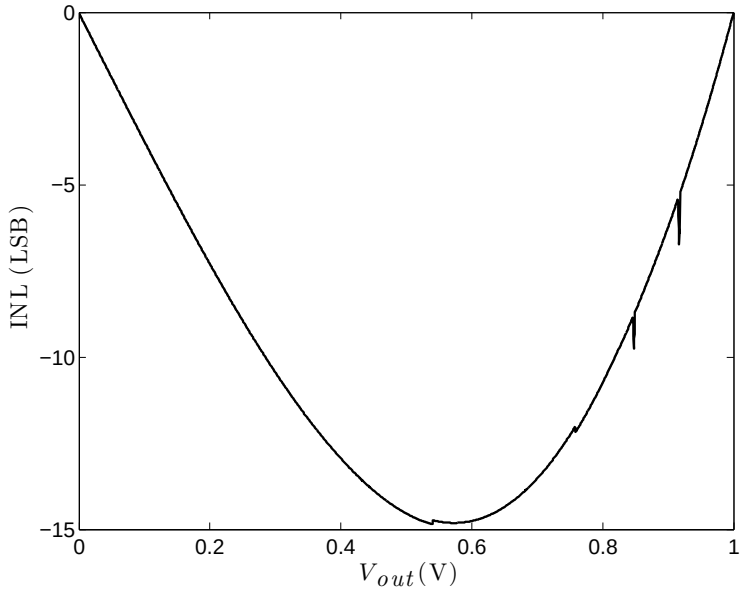

FIGURE 5.10. Filter linearity simulation results, full-scale input range.

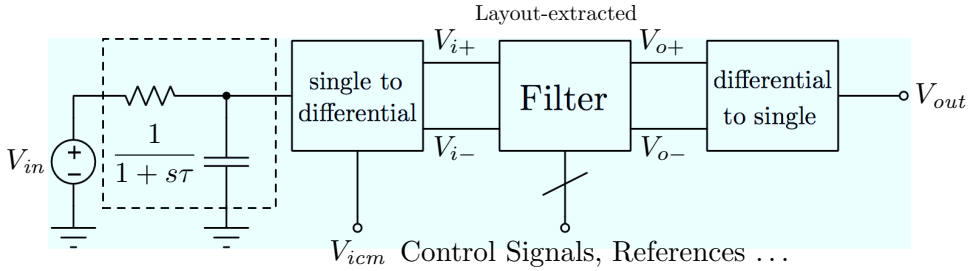

FIGURE 5.11. Weighting function test circuit.

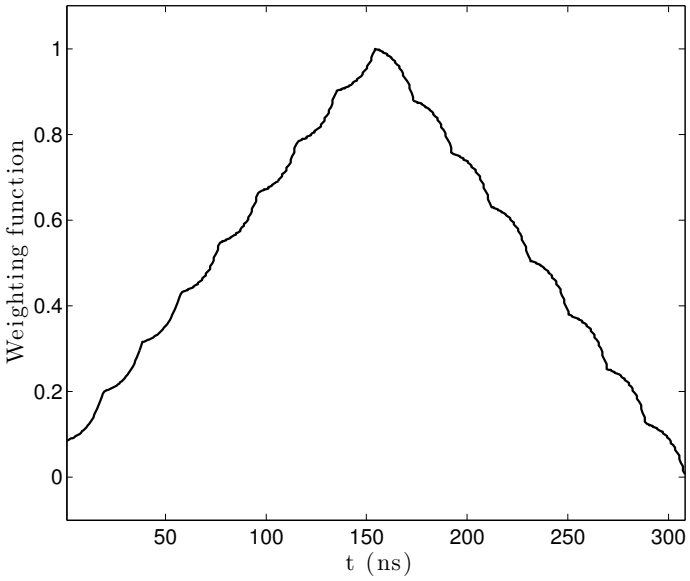

FIGURE 5.12. SPICE-simulated weighting function. $\tau = 8\,\text{ns}$, $N = 16$ and $T_s = 19.25\,\text{ns}$.

6. CONCLUSION

6.1 Summary

This thesis deals with the use of discrete-time filters to process the noise present in particle physics detectors front-end circuits. The main contributions of this work are: the development of a new mathematical framework for a design-oriented analysis of discrete-time filters in the discrete-time domain; and the design and implementation of a switched capacitor (SC) filter for arbitrary weighting function (WF) synthesis to be included in the Bean V2 IC.

One of the most important topics in particle physics instrumentation is finding the optimal WF for noise minimization. Although some WFs, such as the cusp (Radeka, 1968), are impossible to synthesize using continuous-time circuits, it was then interesting to determine the fundamental lower limit of noise that could be achieved through them. From then on, design efforts were focused on synthesizing the closest WFs to these theoretical optimal ones. Once introduced the discrete-time pulse shapers in the early 90's, the design efforts remained on this path, by using discrete-time filters to synthesize WFs similar to the continuous-time optimal WFs. However, this approach ignores the discrete-time nature of the pulse shaper, since taking into account this condition results in different optimal WFs, which for a variety of conditions could be very different to the continuos-time counterparts. This problem leads to the main work presented in this thesis, a mathematical framework to calculate the noise of a typical detector front-end circuit from a discrete-time point of view, and thereby, a powerful tool to design the optimal discrete-time pulse shapers.

From a practical point of view, a generic filter for arbitrary weighting function synthesis is an ideal companion for the theoretical framework mentioned above. The design of this filter was presented in this work, framed on the design of the Bean V2, an application specific integrated circuit (ASIC) planned to meet the BeamCal instrumentation needs. The use of this filter, along with a proper characterization of the CSA and detector

noise statistics, will allow to minimize the output referred noise on the BeamCal front-end circuit.

6.2 Future work

The mathematical framework presented in this work depends on a proper characterization of the CSA and detector noise statistics to find the optimal filter. Once estimated these parameters, the filter coefficients are computed offline, and then, they are updated in the circuit. An interesting future development could be to find a methodology to compute the filter coefficients online without having to characterize the CSA and detector noise statistics separately. To pursue this problem, the mathematical framework presented in this work represents a proper starting point. Also, given the abstraction of this work, it could find applications in other fields with similar circuit configurations, such as the current developments for astronomical instrumentation (Guzman et al., 2013).

The lessons learned during the design and simulation of the Bean filter prototype will prompt corrections, improvements, and upgrades for future revisions. Based just on simulation results, the most urgent correction consist of editing the filter OTA design to meet the settling time specification, and thus, the linearity specification. Filter lab testing are about to start. Additional corrections, improvements, and upgrades are expected as result of this development phase.

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APPENDIX

A. THE BEAN 2 PROTOTYPE PINOUT

The Bean V2 prototype has 48 pads and was bonded to a 64-lead package from Kyocera Corporation (KYO). The package KYO part number is QC064307WZ. The Bean V2 bonding diagram is shown in Fig. A.1. Table A.1 shows the Bean V2 pinout.

Pin number	Pin name	Description
1	AGnd	Analog ground
2	AGnd	Analog ground
3	AGnd	Analog ground
4	NC	No connection
5	NC	No connection
6	res_bias_ext	IC bias external resistor
7	V_ref_prechar	Reference voltage CSA precharger
8	NC	No connection
9	clk_prech1	CSA precharger clk1
10	clk_prech2	CSA precharger clk2
11	NC	No connection
12	op_mode	Operation mode select
13	rst_csa	CSA reset
14	NC	No connection
15	cap_precharge_ext	CSA precharger external capacitor
16	Vin_csa	Vin CSA
17	NC	No connection
18	clk	IC clock
19	AGnd	Analog ground
20	AGnd	Analog ground
21	Vi+_fil	Filter Vi+

Pin number	Pin name	Description
22	Vi-_fil	Filter Vi-
23	NC	No connection
24	Vo-_bp_fil	Filter bypass Vo-
25	Vo+_bp_fil	Filter bypass Vo+
26	NC	No connection
27	DVdd	Digital Vdd
28	DGnd	Digital Gnd
29	NC	No connection
30	Vo-_fil	Filter Vo+ (buffered)
31	Vo+_fil	Filter Vo- (buffered)
32	NC	No connection
33	out_s	Filter output selection
34	Vocm	Filter Vocm
35	hold	Filter hold signal
36	rst	Filter reset
37	sgn	Filter gain sign
38	Vicm	Filter Vicm
39	NC	No connection
40	AGnd	Analog ground
41	NC	No connection
42	NC	No connection
43	CS_b0	Filter CS capacitor bit 0
44	CS_b1	Filter CS capacitor bit 1
45	CS_b2	Filter CS capacitor bit 2
46	CS_b3	Filter CS capacitor bit 3
47	CS_b4	Filter CS capacitor bit 4

Pin number	Pin name	Description
48	CS_b5	Filter CS capacitor bit 5
49	AGnd	Analog ground
50	AGnd	Analog ground
51	Vo+_ch	Channel Vo+ (buffered)
52	Vo-_ch	Channel Vo- (buffered)
53	NC	No connection
54	Vout_csa	CSA Vout (buffered)
55	NC	No connection
56	baseline	CSA baseline (buffered)
57	NC	No connection
58	NC	No connection
59	NC	No connection
60	AGnd	Analog ground
61	AGnd	Analog ground
62	AGnd	Analog ground
63	NC	No connection
64	AVdd	Analog Vdd

TABLE A.1. The Bean 2 prototype pinout

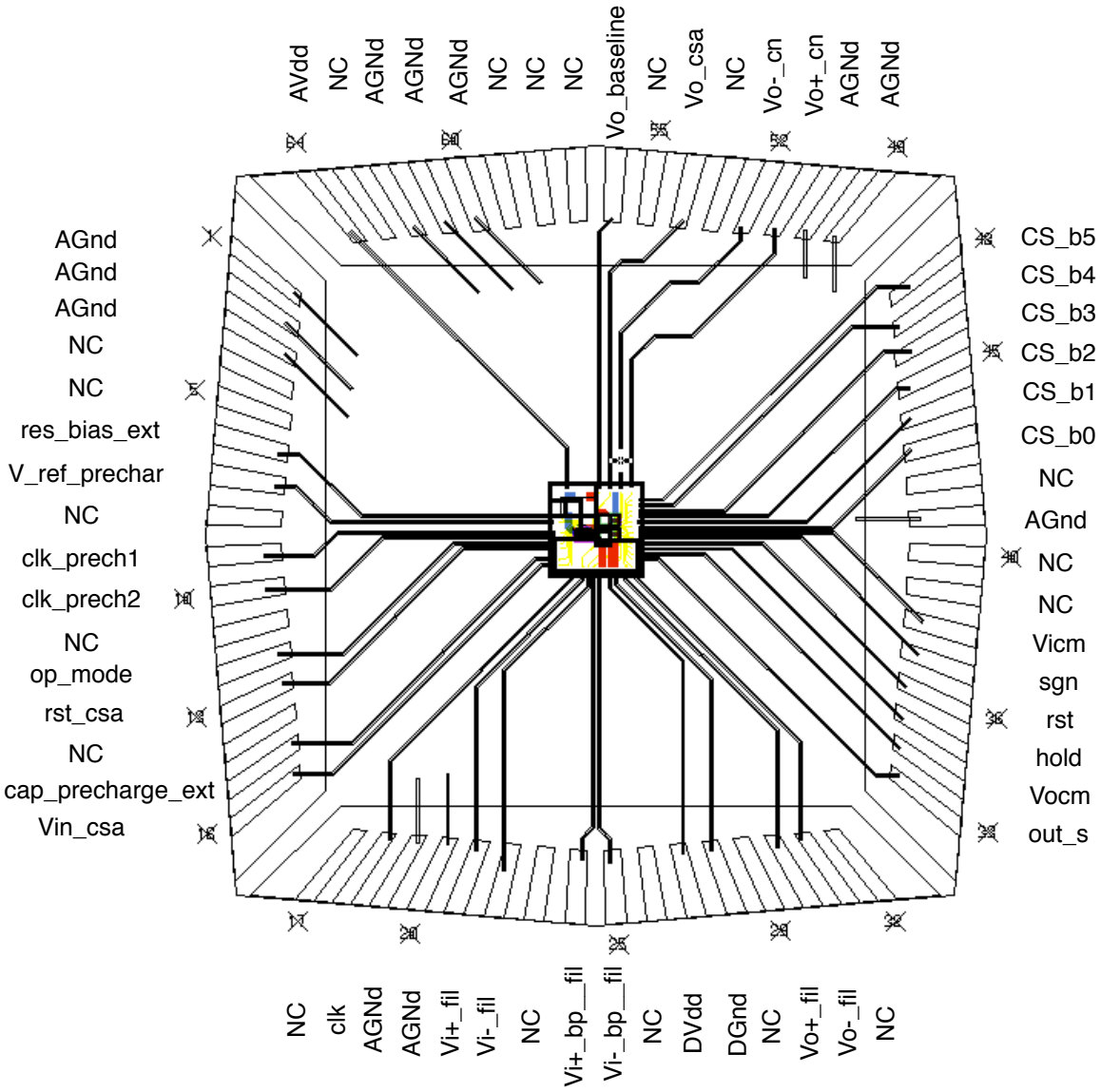

FIGURE A.1. The Bean 2 prototype bonding diagram.