2T1M-based double memristive crossbar architecture for in-memory computing

Abstract

The recent discovery of the memristor has renewed the interest for fast arithmetic operations via high-radix numeric systems. In this direction, a conceptual solution for high-radix memristive arithmetic logic units (ALUs) was recently published. The latter combines CMOS circuitry for data processing and a reconfigurable “segmented” crossbar memory block. In this paper we build upon such a conceptual design and propose a 3D extension of the classic crossbar topology via 2T1M cross-points which still permits the parallel creation of partial products for faster multiplication with lower circuit complexity. Furthermore, we present a binary to high-radix data conversion circuit to complement the stateprogramming module of the previous work. A simulation-based validation of read/write multi-level memory operations from/to the 2T1M 3D memristive crossbar was performed using SPICE and a thresholdtype switching model of a bipolar voltage-controlled memristor. Such realization of in-memory computations could lead to faster arithmetic algorithms in future memristive ALUs..

Keywords

Memristor, Memristive system, Resistive switching, Nanoelectronics, Crossbar, Resistive random access memory, High-radix arithmetic, SPICE, Parallel computing.